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-filed July 23, 1999

Re: Application of Vitaly A. VOLODIN
DRIVING METHOD, DRIVING DEVICE FOR DISPLAY, AND DISPLAY (VARIANTS)
Our Ref: Q62631

Dear Sir:

The following documents and fees are submitted herewith in connection with the above application for the purpose of entering the National stage under 35 U.S.C. § 371 and in accordance with Chapter II of the Patent Cooperation Treaty:

☑ an executed Declaration and Power of Attorney.

☑ an English translation of the International Application.

☑ twenty-five (25) sheet(s) of drawings.

☑ Notification Concerning Submission or Transmittal of Priority Document.

The Assignment will be submitted at a later date.

It is assumed that copies of the International Application, the International Search Report, the International Preliminary Examination Report, and any Articles 19 and 34 amendments as required by § 371(c) will be supplied directly by the International Bureau, but if further copies are needed, the undersigned can easily provide them upon request.

The Government filing fee is calculated as follows:

Total claims	19	-	20	=		x	$18.00	= $.00
Independent claims	10	-	3	=	7	x	$80.00	= $560.00
Base Fee								$1000.00
TOTAL FEE								$1560.00

A check for the statutory filing fee of $1560.00 is attached. You are also directed and authorized to charge or credit any difference or overpayment to Deposit Account No. 19-4880. The Commissioner is hereby authorized to charge any fees under 37 C.F.R. §§ 1.16, 1.17 and 1.492 which may be required during the entire pendency of the application to Deposit Account No. 19-4880. A duplicate copy of this transmittal letter is attached.

Priority is claimed from August 03, 1998 based on Russian Application No. 98114874.

Respectfully submitted,

Darryl Mexic
Registration No. 23,063

DM/amt

DRIVING METHOD, DRIVING DEVICE FOR DISPLAY, AND DISPLAY (VARIANTS)

FIELD OF THE INVENTION

The invention relates to electronics, microelectronics, flat displays, methods and apparatus for driving liquid crystal displays (LCD), computer and television facilities, and to other fields of engineering where the flat displays are used.

BACKGROUND OF THE INVENTION

A driving method, a device for driving an LCD, and the LCD are known.

The known display of direct [US Patent N 5,099,435] or projective [US Patent N 5,465,102] type contains an LC panel. The panel contains, at least, two transparent substrates non-conducting a current, located one opposite another and having a gap between them. The gap is filled with LC material, e.g., nematic of which compositions and formulae are known [US Patents NN 5,099,345; 5,262,881]. The LC material specifically oriented turns a direction of polarized light transmitted from the substrate side at the angle depending on root-mean-square (rms) voltage applied to the LC material.

The voltage to the LC material is applied from the side of optically transparent and electrically conducting electrodes disposed on the inner surface of the substrates. The electrodes of one substrate called as row- or scanning- or common- or Y-electrodes are located crossly to the electrodes of another substrate called as column- or signal- or segment- or X- electrodes. There are formed LC cells in the layer of LC material between the scanning and signal electrodes at their intersection points.

The LC cell in conjunction with some other elements, e.g., polarization films, color or other filters, glasses or films compensating color distortion and expanding viewing angle, sets an elementary display cell and a "dot" display image element called a "pixel". The brightness of the pixel is driven by voltages on the LC cell electrodes.

Nematic molecules twisted at angles from 90° (or 180°) to 360° [T.J. Sheffer and J. Nehring, Appl. Phys. Lett., v.45, N10, pp.1021-1023, 1984] are called "super twisted nematic (STN) molecules". STN LC cells allow to create passive-matrix (PM)

LC panels with a great number of multiplex scanning electrodes having a sufficient number of rows to realize computer and television dual scan displays.

A section of a PM LCD panel in plan is represented in FIG.1. The signal electrodes are denoted by X_1, X_2,...,X_j,..., X_M, the scanning electrodes are denoted by Y_1, Y_2,...,Y_i,...,Y_N. Voltages are applied to the display electrodes from row and column drivers.

The PM LCD is driven by various methods based on sequential selection of display row electrodes. The row electrodes are selected in one-by-one or group-by-group sequence. Scanning voltages are applied to the selected electrodes and a reference voltage to the non-selected electrode. Voltages setting values of brightness of display elements are applied to the column electrodes.

In order to determine display characteristics, rms voltage values at the electrodes of the LC cells, and diagrams of driving voltages, the electro-optic behavior (EOB) of the display element is used.

The variants of the EOB of the display element in the form of a voltage-brightness characteristic (VBC) are given in FIG.2 and FIG.3. U_{ij} is the rms voltage on an (ij)-LC cell placed between i-row and j-column electrodes. B is a brightness of the pixel connected with the (ij)-cell. The work region of the VBC is a steep region bounded on the values of the brightness B_{min} and B_{max}. The brightness is measured in Kd/m^2. The ratio B_{max}/B_{min} determines the maximum display contrast of the display. The work region is characterized by two main rms parameters as well. The first one is the threshold voltage U_{th} on the VBC shown in FIG.2, identifying the off-boundary state setting B_{min}, and denoted as well by U_{off}, hence $U_{off}=U_{th}$. The second one is the transition voltage Δ giving, after adding to U_{th}, the on-boundary state denoted by U_{on} and setting B_{max} on the VBC shown in FIG.2, hence $U_{on}=U_{th}+\Delta$. The rms values between U_{th} and $U_{th}+\Delta$ specify intermediate values of the brightness (a scale of gray). In FIG.3, U_{off} sets B_{max} and U_{on} sets B_{min}.

The first prototype of the invention is the Alt-Pleshko method to drive the PM LC display by one-line addressing, described as a prototype in US Patent N5,162,923.

The timing diagrams of the first method are shown in two figures, under absence of pulse width modulation (PWM) of column signals (FIG.4) and under the

PWM of column signals (FIG.5) to set "gray scale". In both figures V_{ri} and V_{cj} denote voltages applied to i-row and to j-column electrodes, $V_{ij}=V_{cj}-V_{ri}$ is a voltage applied to ij-electrodes of the LC cell. Inscriptions "On", "Off" or "Gray" in these and others figures denote a brightness of the pixel being related to the selected cell. The term "gray" implies the brightness level different from "On" and "Off".

The method consists in selecting scanning electrodes in sequence one by one. During a selection period T_r of a constant duration, a scanning voltage V_r (a row pulse) having a constant magnitude of deviation from some reference voltage V_0 is applied to the selected scanning electrode, the reference voltage is applied to the non-selected scanning electrodes, a signal voltage level or voltage levels (column pulses) unequal to Vo-level and having, in general case, variable durations are applied to a signal electrode to set current values of brightness of a selected display element.

During a frame time period $T_F = NxT_r$, the row pulses are applied to all N scanning electrodes of the display. After every some time period, polarities of both row and column pulse deviations (about V_0-level) are reversed, thereby a zero mean value of the voltage applied to LC cell is provided. In order to reduce supply voltage, every reversing of the polarities is accompanied by change of the reference voltage V_0 from V_{01} to V_{02} or from V_{02} to V_{01}, in opposition to the change of the row pulse deviation.

At every instant, the reference voltage V_0 (V_{01} or V_{02}) is applied to the N-1 non-selected row electrodes. It is kept on a row electrode, during a frame time, in the course of $(N-1)T_r$. If the polarity of the level V_c about V_0 is different from the polarity V_r, the state "On" is set, therefore such level is denoted by $V_c(on)$. Accordingly, the level V_c having polarity equal to the polarity V_r is denoted by $V_c(off)$. Durations of both $V_c(on)$ and $V_c(off)$ pulses, respectively t_{on} and t_{off}, can be established variable (under PWM), each being changed from 0 to T_r depending upon the information to be displayed. However their total duration must be equal to the selecting time T_r, i.e. $t_{on}+t_{off} = T_r$.

On the other hand, a frame modulation method is widely used to form the gray scale. The method consists in applying, during several frames, voltage combination $V_c(on)$ and $V_c(off)$, each voltage having constant duration equal T_r, to the selected LC

cells. This method is a prototype of the invention as well. The terms "frame" and "field" are often used as synonyms. We refer the term "field" to the time of single selection of all display pixels and the term "frame" to the time of single applying full information about brightness of all pixels. (So, instead of "frame modulation" the term "field modulation" should be more relevant since the information about gray brightness for the pixels is applied to signal electrodes in course of four or eight fields of a frame. However the term "frame modulation" is used here as generally accepted).

The rms voltage on the ij-cell is set by multiple (several tens) applying of row pulses to the i-th row electrode and of column levels of constant or variable durations to j-th column electrode.

The parameters of the PM LC driven by the method-prototype and the values of row and column pulses are determined using VBC of the cell and relying upon the theory by Alt & Pleshko [Alt P.M., Pleshko P., IEEE Trans. Electron Devices, v.ED-21, N2, pp.146-155,1974].

Alt and Pleshko introduced the constructive parameter $p = \Delta/U_{th}$ representing the measure of non-linearity of the EOB. Parameter p allows to find the LC-cell parameter N_{max} defined exactly by expression:

$$N_{max} = [(1+p)^2+1]^2/[(1+p)^2-1]^2 \qquad (1)$$

determining the maximum number of multiplex row electrodes.

Under small p (large N_{max}), the expression (1) goes to the simple form:

$$N_{max} \approx 1/p^2 = U_{th}^2/\Delta^2 \qquad (2)$$

According to Alt and Pleshko, the maximum scanning opportunity is realized in the LCDs satisfying the equality:

$$N_{max} = N \qquad (3)$$

Each of satisfying to (3) LC display cell are to be supplied by pulses of voltage, which modulus of deviation from reference voltage V_0 satisfies to

$$V_r = \frac{U_{th}}{2}\,\frac{[(1+p)^2+1]^{\frac{3}{2}}}{(1+p)^2-1},$$

or, taking into account (1), (3), and small p,

$$V_r = \frac{U_{th}}{\sqrt{2}}\sqrt{N} \qquad (4)$$

In a similar way, the column electrodes must be supplied by voltage level:

$$V_c = \frac{U_{th}}{2}\sqrt{(1+p)^2+1},$$

or, for small p,

$$V_c = U_{th}/\sqrt{2} \qquad (5)$$

To characterize relationship of driving voltages they use a parameter "bias ratio" defined as $b = V_c/(V_r-V_c)$ for the state "On":

$$b = 1/(N^{1/2} + 1) \qquad (6)$$

The deficiency of the known method is an insufficient contrast and a small operation speed with compare to AM LC display. Sparse row pulses of large amplitude give rise significant oscillations in orientation of LC molecules, hence, the fluctuations of light and optical characteristics of display pixels about the state determined by rms voltage at the LC cell. This is explained by time diagrams FIG.6 corresponding to voltage-brightness characteristics of FIG.2 and FIG.3. The rms voltage levels U_{th} and $U_{th}+\Delta$ for the states "On" and "Off", set by row and column voltages are denoted by dotted lines on both time diagrams FIG.6. Module of current difference $|V_{cj} - V_{ri}|$ producing the states "On" and "Off" is shown on the upper time diagram. In the low diagram, solid line follows a value of some parameter of the cell, named as "quasi-rms" voltage. Each of quasi-rms voltage value corresponds to certain spatial orientation of LC molecules that could take place in LC cell under voltages of the constant module on the electrodes of the LC cell. The oscillations of spatial orientation of LC molecules under action of row and column voltages and brightness fluctuations can be estimated from the shapes and magnitudes of quasi-rms voltage oscillations at the cells. The parameter "quasi-rms voltage" is characterized by such notions as "relaxation time" and "response time", unlike the parameter "rms" being just a result of mathematical procedure of averaging. (Further for calculation of transient process, the notion "quasi-rms voltage" is replaced with the notion "quasi-mean square voltage").

The stationary quasi-rms voltage oscillations under finite value of relaxation time of LC molecules cause fluctuations of light and optical states of display pixels. During a relaxation time, a small number of driving cycles cause large quasi-rms voltage oscillations, fluctuations and blurring in pixel brightness. The quasi-rms voltage fluctuations around levels "On" and "Off" cause darkening of "white" or lighting of "black" images and decrease the image contrast and brightness. This phenomenon is called "a frame response" effect.

Large relaxation time during which the electrodes supplied by great number of driving cycles provides decrease of quasi-rms voltage oscillation magnitudes and increase of the contrast at the cost of speed response reduces.

The "fast" display should be driven by the pulses of high frequency. However, the shapes of high frequency pulses, both row and columns, are distorted along RC line electrodes. Because of LC cell capacitance, mutual influence of signals from various electrodes (cross-talks) is pronounced at high frequencies. Both effects being correlated to some extent cause a distortion of rms voltage at LC cell electrodes, an unevenness of brightness and contrast over the display area, and distortions of the image in structure, fragments and of colors.

The effects of long lines with distributed capacitance and resistance limit a development of the displays with large dimensions and high quality of the image, not only for passive-matrix displays, but for active-matrix ones as well. Control of the mentioned effects is out of the subject of PM LC displays.

The intermediate values of relaxation time for LC materials used in PM LC displays driven in known methods allow to develop the cheep (relative to AM LC) displays being, however, deficient in speed, contrast, and brightness of the image. The methods to control a spurious effect of the frame response, signal distortions and electrodes coupling are known. The methods described below are discussed as the other prototypes of given invention.

The second prototype of the invention is the US patent N 5,301,047 (Hitachi) on variants of a method to reduce effect of driving pulse distortions when the pulses (under one-line addressing) propagate down long electrode. The variants are based on formation of high-frequency voltages of various forms being added continuously to

either the row, or column, or row and column voltage levels. The aim of the method is to improve the uniformity of the image displayed.

An example of the shape of resulting voltage V_{ij} at ij-cell produced by superimposing continuously chopping wave to row and column driving voltages is shown in FIG.7.

A positive effect of the method is due to decrease of magnitudes of high frequency harmonics of the pulses applied to the electrodes because of the pulses with steep edges (fronts and tails) have been smoothed by adding of compensating voltages, and due to reduce of their filtration level.

However, the method provides no essential increasing an operation speed, since formation of additional compensating higher frequency voltages gives rise to higher frequency harmonics in a spectrum of the driving pulses, and to degradation of the image. On the other hand, superimposing the said additional signals hinders a formation of gray scale using the WPM.

The third prototype of the invention is US patent N 5,162,932 (Matsushita) on a method for one-line driving the PM LC display, the method allowing to decrease distortions of column driving signals when the pulses propagate down long the column electrode. To get effect, the selecting voltage V_r of duration T_r smaller than duration of row selecting period T_s is applied to the row electrodes. Additional levels V_c(on) and V_c(off) are allocated to a beginning and to an end portions of the scanning period T_s, the allocations are reversed at intervals of succeeding scanning periods.

Aforesaid is explained by diagrams of row and column voltages (FIG.8). Voltages V_{ri} and V_{cj} are applied, respectively, to i-th and to j-th column electrodes of the display. The voltage V_{ij} is formed on the ij-cell electrodes. V_{01} and V_{02} are the reference voltages in succeeding frame periods. Additional levels are come in time interval T_s and out off the T_r, that is within time interval T_s-T_r.

As from the diagram follows, under any pixel brightness ("On", "Off", or "Gray") the number of voltage changes from V_c(on) to V_c(off) and vice versa in the course of selection time T_s becomes equal to one (with compare to two changes in time interval T_r for any of "Gray" states of FIG.5). Hence, the method enables to

reduce to one-half the number of V_c-voltage changes and the value of laying induced on electrodes by voltage changes.

However, a decrease of row selecting pulse duration T_r with compare to row selection period T_s leads to increase of row pulse magnitudes in T_s/T_r times. As a result, a contribution of distortion of the pulses to the square of quasi-rms voltage fluctuation increases $(T_s/T_r)^2$ times.

The forth prototype of the invention is US patent N 5,151,690 (Seiko Epson) on a method for one-line driving PM LC display. In addition to the time interval during which the driving voltages are applied to the display electrodes ("the driving times"), there is a period of time ("the compensation time"). During the period of compensating time, signal electrodes are energized by an additional voltage necessary for at least partial compensation of distortions caused by changes of image in the earlier period. The compensation voltage are set in accordance with the number of variations between "on" and "off" states on a column electrode for the previous period of a time preceding the compensating time. During additional time interval, all the row electrodes are supplied by the reference voltage. The method enables to decrease image uniformity arising because of distortions of column voltage changes from V_c(on) to V_c(off) and vice versa.

Aforesaid is explained by diagram of row and column voltage (FIG.9). The voltages V_{ri} and V_{cj} are applied to, respectively, i-th row electrode and j-th column electrode of the display, voltage V_{ij} is applied to ij-electrodes of the cell. V_{01} and V_{02} are the reference voltages in succeeding frame periods. Driving voltages are applied to display electrodes within frame time interval T_F in accordance with the first driving method discussed. After completing the period of selection of all row electrodes, the column electrodes are fed, during the additional time t_c, by voltages depending on display pattern.

The weakness of this method is the limitation in efficiency. At best, a maximum distortion of image brightness may be reduced only by half at the expense of arising the added distortions the same magnitude and opposite polarity at other places undistorted before.

The fifth prototype of the invention is US patent N 5,157,387 (Seiko Epson) on a method for one-line driving PM LC display. The aim of the method is the generation of substantially homogeneous cross-talks noise over the entire display. The task is solved by applying, during period T_r, two voltage levels to column electrode, the voltage of one (high) level being applied for a primary time interval and the voltage of the other (low) level for the secondary time interval. The relative duration of the primary and secondary intervals determines the contrast gray level of the pixel.

Timing diagram of driving voltages formed in accordance with the fifth prototype are shown in FIG.10 and FIG.11. The timing diagrams for row voltages V_{ri} (FIG.10) are not different from the similar diagrams of the first method-prototype (FIG.4). A distinction of the diagrams for column voltages V_{cj} (FIG.10 and FIG.11) from the diagram V_{cj} in FIG.5 is applying, during the selection interval T_r, additional voltage level of several types.

Variants of the diagrams of column voltage (V_{cj1}, V_{cj2} and V_{cj3}) without PWM are given in FIG.10.

An additional level of the diagram V_{cj1} is the reference voltage, V_{01} or V_{02}, applying to the column electrode after applying the basic ("On" or "Off") level. An additional level on the diagrams V_{cj2} and V_{cj3} is the level of opposite deviation about the reference voltage with respect to the basic ("On" or "Off") level. The additional levels on diagrams V_{cj1} and V_{cj2} are always allocated to the end of T_r interval (in the moments t_1) marked by arrowed lines in FIG.10. Additional level "On" on diagram V_{cj3} is always allocated to the end of T_r interval in the moments t_2, and additional level "Off" is always allocated at the beginning of T_r interval in the moments t_3. The levels t_2 and t_3 are marked by arrowed lines as well.

Under using the PWM method, two voltage levels are applied to column electrode in the time interval T_r. Unlike PWM driving of the first method, one of the levels is allocated to the center of the time interval T_r while another is before and after the said interval. FIG.11 shows eight variants of the diagram for V_{cj} forming eight brightness gradations. One more distinction of the PWM method discussed is a presence of a second voltage level on the diagrams for brightness levels "On" and "Off" (on the first and the last diagrams in FIG.11).

However, the method does not provide a valuable reduce of the rms distortions. According to the method, a portion of duration for each of said values is varied regardless of duration of additional voltage level. The given method used to a display designed to the Alt & Pleshko method can lead to decrease of the image contrast.

The sixth prototype of the invention is a one-line method of driving PM LC display by means of amplitude modulation forming "gray scale" gradations. The method is offered by T.N. Ruckmonganthan in [JAPAN DISPLAY'92, pp.77-80]. Brightness value is represented by value k, where k varies from -1 to +1 over a range of pixel brightness. Column electrode is fed twice during time interval T_r of pixel selection. The information voltage is specifically transformed so that, at first half of interval T_r, the electrode is fed by voltage $(k+\sqrt{1-k^2})V_c$, while at second half of the interval by voltage $(k-\sqrt{1-k^2})V_c$, where V_c is a module of voltage deviation from the reference level V_0 for the case of Alt & Pleshko addressing.

An advantage of Ruckmonganthan's method is a constant duration of driving signal level for any "gray" level, unlike the PWM-method where duration of driving level can be too small. Therefore Ruckmonganthan's method is enhanced in a speed.

A weakness of the Ruckmonganthan's method is a variable value of voltage changes applied to column electrodes in a frame period. Their distortions limit a possibility to improve the image quality and speed of displays.

The seventh prototype of the invention is US patent N 5,093,736 (Seiko Epson) on a method for one-line driving PM LC display having a big number of scanning electrodes (no less than 300). The aim of a method is to increase the image contrast and speed of the display. The highest contrast of the display have been reached by variation of driving voltage in the displays having a number of scanning row electrodes up to 500. The displays have been manufactured using various LC compositions with molecules twisted from 240° to 300°. The row and column electrodes are fed by driving voltages having the "bias factor" b, unlike (6), not equal to $1/(N^{1/2}+1)$, in the range from $1/(N^{1/2}-N/200)$ to $1/(N^{1/2}-N/50)$.

However, this method offers no way to create high speed PM LC display. Result is unexplainable by the Alt & Pleshko theory indicated an incompleteness in the knowledge of the diving theory.

The eighth prototype of the invention is US patent N 5,489,919 (Asahi Glass Company) on a method for multiple-line driving PM LC display. Scanning electrodes are selected by group. Selected electrode of a group is fed by scanning voltages ($+V_{ro}$ or $-V_{ro}$) accordingly to certain order specified for a given sort of selection. The said order provides applying selection voltages to the same row electrodes simultaneously selected several times in a frame (e.g., two, four, four times a frame under two-, three- and four-row selection, respectively, and so on). The reference voltage of constant value is applied to non-selected row electrodes.

The groups of the voltage applied to the selected row electrodes during the frame period are considered as the column voltage vectors, and may be shortly described by Hadamard's matrix of which the values +1 and -1 corresponds to, respectively, $+V_{ro}$ and $-V_{ro}$. The other forms of matrix representation are available. For example, the matrix in which the value -1 denoting the voltage $-V_{ro}$ is replaced by 0.

The group of four time diagrams for voltage V_{r1}, V_{r2}, V_{r3} and V_{r4} applied to four row electrodes selected simultaneously is shown in FIG.12 (one of possible variants). On the diagrams, the change of voltage polarity relative to the reference level V_{01} in two frames is shown, the change providing a zero mean voltage at the display cells. The frame comprises four fields, each being of duration T_{fld}. Duration of a selective action is T_r. The matrixes of two said types corresponding to time diagrams in FIG.12 are given in FIG.13.

Depending on brightness of the pixels placed at intersection column electrode with row electrode group selected, the column electrode is fed by the voltage calculated in accordance with the certain procedure. Following this procedure, a column electrode is fed by the voltage proportional to the sum of values obtained for each pixel from the selected ones by the action of the algorithm -"exclusive-or" under both logical values (corresponding to the brightness of the pixel selected) and the

logical value corresponding to polarity of the selecting voltage applied to the row electrode of this pixel (right matrix in FIG.13).

Assume that at some moment four j-th column pixels having the brightness values (e.g., on, on, off, off) corresponding to brightness logical values, respectively, (1,1,0,0) called "data", are selected. When the voltages are applied to selected row electrodes in accordance with some current column of the right matrix (FIG.13), e.g., the first one having the column values (1,1,1,1), the driving voltage is synthesized to be proportional to the said sum $1\bullet1+1\bullet1+1\bullet0+1\bullet0=2$ denoted by symbol **i**, where the sign • denotes "exclusive or" function. In similar way, in the next field at the moment of selecting these pixels (with the same data), when the second group of driving voltages described by the values (1,0,1,0) are applied to the row electrodes, the column voltage is synthesized proportionally to $\mathbf{i}=1\bullet1+0\bullet1+1\bullet0+0\bullet0$ since $0\bullet0=1$. In a frame period such each carries out four times.

The value of the column voltage is proportional to integer **i** ranged from 0 to 4 for four-row selection, or from 0 to L for L-row (L-pixel) selection. The values of voltage applied at the current moment to the column electrode is defined by $V_c(2i-L)/L$, where the value V_c the authors of the prototype of the invention call "the maximum value of column electrode voltage".

Each brightness combination of the selected pixels is produced as a result of a multiple feed of the voltages synthesized following the said procedure.

The aim of the method is reducing the frame response effect, i.e. increasing the uniformity and the contrast of the image, display dimensions and operation speed.

However, the method gives no way to create sufficiently fast-speed displays. Analysis shows that the frame response under four-line addressing does not decrease frame response under specific types of pattern . If four-line addressing uses row selection of type shown in FIG.12, the frame response increases up to the one-line addressing level for 50% of brightness pattern: (1,1,1,1), or (1,1,0,0), or (1,0,1,0), or (1,0,0,1), or (0,0,0,0), or (0,0,1,1), or (0,1,0,1), or (0,1,1,0). Besides, the displays designed to work on this driving method with four-line addressing can be disabled under the three-line or seven-line ones.

Discussed above, the voltage pulses corresponding to particular method are usually formed by row and column driver chips. The clock pulses and signals containing the pixel brightness information are fed to drivers from a controller device operating with (or comprising) RAM and ROM. Supply voltages are fed to drivers, controller and other devices from the power supply. Driver block-diagrams and circuit peculiarities of the devices performing the aforesaid method are given in the patent cited.

DISCLOSING OF THE INVENTION

Suggested variants of the driving method, the driving device for LC displays, and the LC display driven by them are based on the theory deepening the Alt - Pleshko theory. For understanding of the invention subject, proof its feasibility and positive effect, the theory is briefly described.

Theoretical background

1). The usual electro-optic behavior (EOB) of an (ij)-image element of LCD in the form of a voltage-brightness characteristic (VBC) is given in FIG.2 and FIG.3.

Our theory is based on constant use of a concept of a mean-square (ms) voltage instead of the rms voltage and on a square voltage – optic characteristic as the EOB (see EOB in the form of square voltage – brightness behavior in FIG.14). The boundary parameters of the work region U_{th1}^2 are U_{th2}^2 are introduced instead of U_{th}, $U_{th}+\Delta$, and Δ. It is introduced the parameters of work region $U_{gr}^2=(U_{th2}^2+U_{th1}^2)/2$ (a middle point, a work point of the work region, "gray level"), and $D=U_{th1}^2-U_{th2}^2$ (the width of the work region).

As applying the voltage pulses causes the frame response effect in LCD, we introduce the notion quasi-mean square voltage (quasi-ms voltage) of the LC cell to study this phenomenon. Each current momentary value of the quasi-ms voltage of the LC cell is a mapping of a current momentary LC molecule's direction and is equal to the value of the ms voltage setting the same static direction of the LC molecules of the same LC cell. The notion of the quasi-ms voltage makes possible to study transient process in the LC cell, calculate oscillations of image element brightness under action of row and column voltages. Unlike the parameter "ms voltage", the notion "quasi-ms voltage" is characterized by time characteristics "relaxation time",

"response time", etc. In addition to the static EOB shown in FIG.14, we introduce a dynamic EOB representing changes of brightness depending on frame frequency. Two types of EOB, static and dynamic, are shown in Fig.15 where the brightness B plotted as a function of ms voltage and averaged quasi-ms voltage respectively. The static curve shown in FIG.15 by dotted curve, dynamic one is shown by solid curve. In Fig.15 it is shown the stationary oscillation of the quasi-ms voltage about its average value giving rise to shift of static threshold values, $<U_{th1}>^2$ to $<U_{th3}>^2$ and $<U_{th2}>^2$ to $<U_{th4}>^2$. The value $<Ugr>^2$ is varied a little.

FIG.15 allows estimating the value of the contrast drop from $K=B_{max}/B_{min}$ to $K_1 = B_{max1}/B_{min1}$.

2). The constructive parameter $P=D/U_{gr}^2$ is set instead of p.

The LCD parameter $N_{max}\equiv(U_{th1}^2+U_{th2}^2)^2/(U_{th2}^2-U_{th1}^2)^2$ of the LC cell are written exactly as $N_{max}\equiv 4/P^2\equiv 4U_{gr}^4/D^2$.

The parameters $<U_{gr}^2>$ and D allow to calculate the LCD parameter N_{max}:

$$N_{max} = 4<U_{gr}>^4/(<U_{th2}>^2 - <U_{th1}>^2)^2 \qquad (7)$$

exact as well as (1) and simple as well as (2).

The other form

$$N_{max} = <U_{gr}>^2/\Delta^2 \qquad (8)$$

has the accuracy better $4\sqrt{N_{max}}$ times in comparison with (2).

3). We claim that any method setting the ms voltage on LC cell is correct if the ms voltages set by the method are within the work band of the cell including the boundaries and are not out of the work band.

Label $\min(N_{max})$ required for correct addressing LCD by N_o.

It follows from (3) that for case of one-line addressing $N_o = N$.

The theoretic analysis shows that LCDs having LC cells satisfying the $N_{max}>N_o$ can be driven correctly by one-line addressing and by other methods.

Label values of driving voltages V_r and V_c by V_{ro} and V_{co} for any correct addressing LCD having $\min(N_{max}) = N$ or $\min(N_{max}) = N_o$. After replacing such LCD with LCD having $N_{max} > N$ or $N_{max} > N_o$, the magnitudes of correct driving voltages must satisfy two types of sets of simultaneous equalities:

$$V_r = V_{ro}\sqrt{1+\sqrt{1-\xi}}\ ,\ V_c = V_{co}\sqrt{1-\sqrt{1-\xi}} \quad (9)$$

$$\text{or } V_r = V_{ro}\sqrt{1-\sqrt{1-\xi}}\ ,\ V_c = V_{co}\sqrt{1+\sqrt{1-\xi}}\ , \quad (10)$$

where $\xi = \min(N_{max})/N_{max}$ (that is $\xi = N/N_{max}$ or $\xi = N_o/N_{max}$), V_{r0} and V_{c0} are the driving voltage modules for the displays having $N_{max} = N$.

We can write expressions (9) and (10) in the forms:

$$V_r = V_{ro}\sqrt{1+\eta}\ ,\ V_c = V_{co}\sqrt{1-\eta}\ , \quad (11)$$

$$V_r = V_{ro}\sqrt{1-\eta}\ ,\ V_c = V_{co}\sqrt{1+\eta}\ , \quad (12)$$

where

$$\eta = \sqrt{1-\xi} \quad (13)$$

Vice versa, a display in which the most contrast is achieved due to application of the voltages V_r and V_c different from (4) and (5) introduced by Alt and Pleshko or with bias coefficient b unsatisfying the expression (6), has in fact a value N_{max} satisfying an equality

$$N_{max} = N/(1-\eta^2), \quad (14)$$

where η is non-unit.

For instance, US patent N 5,093,736 (the seventh prototype of the invention) defends the method of one-line addressing in the displays having a number $N \geq 300$ of multiplexed electrodes and the bias ratio b whose value is determined in the range from $1/(N^{1/2}-N/200)$ to $1/(N^{1/2}-N/50)$.

The authors consider that this range provides the high value of the contrast. From analysis, however, it follows that an image quality increase is only possible for LC display with constructive parameters specifying the value N_{max} being a fixed times (from 1.026 to 1.4 for $N = 400$ in the mentioned range of b) greater than the number of electrodes. Other displays with smaller or larger values N_{max} are out of reaching the high contrast for the value b varying in the mentioned range, despite a use of great number of the electrodes $N \geq 300$. In order to achieve the high contrast values for the displays with N_{max} fitting the mentioned range of b, it takes the correct driving provided by the driving voltage modules generation accordingly to (10) or (12).

Taking into account quasi-rms oscillations (see FIG.15), it is necessity to increase the static value N_{max} additionally.

4). The expressions (4) and (5) for row and column voltages in term U_{gr} (without regard to the polarities) under classic one-line addressing are written:

$$V_r = U_{gr}\sqrt{N}/\sqrt{2} \quad (15)$$

$$V_c = U_{gr}/\sqrt{2} \quad (16)$$

Such type expressions under classic two-line addressing (without regard to the polarities):

$$V_r = U_{gr}\sqrt{N}/2, \quad (17)$$

$$V_c = U_{gr}, \text{ and/or } V_c = 0. \quad (18)$$

Under classic multiple-line addressing with any integer L of simultaneously selected row electrodes:

$$V_r = U_{gr}\sqrt{N/2L}, \quad (19)$$

$$V_c = U_{gr}\sqrt{L/2}, \text{ and/or} = U_{gr}\sqrt{L/2-1}, \text{ and/or} = U_{gr}\sqrt{L/2-2}, \quad (20)$$

and so on up to $V_c=0$ if L is even or up to $U_{gr}/\sqrt{2}$ if L is odd.

The number of possible magnitudes of V_c is equal to L/2+1 if L is even and is equal to (L−1)/2+1 if L is odd. Taking account of the voltage polarities, the number of possible V_c levels is equal to L+1.

Note that the MLA having L equal to two to power integer (2, 4, 8, ...) requires to use LCDs having minimum value N_{max} = N. In all other cases, $\min(N_{max})>N$. For L=3 for example, $\min(N_{max}) = 1.33N$.

5). At increased frame frequencies, the frame response is increased but the image quality is impaired because of pulse shape distortions of the row and column voltages propagated along the row and column electrodes.

For rectangular pulse applied to the electrode in the absence of cross-talks, the rms square $\langle U_{ij}\rangle^2$ at (i,j)-th cell can be written as

$$\langle U_{ij}\rangle^2 = \langle U_{gr}\rangle^2 [1 + I(i,j)/\sqrt{N_{max}}]\cdot[1 - \tau_r(j)/T_r - \tau_c(i)/T_r], \quad (21)$$

where I(i,j) is a numerical value of brightness of (ij)-th pixel within working range (steep region in FIG.15), varying between -1 and +1,

$<U_{gr}>^2 [1 + I(i,j)/\sqrt{N_{max}}]$ is a (i,j)-th cell current value of the quasi-ms voltage within working range of the ms voltage (steep region in FIG.15) without regard to distortions,

$\tau_r(i)$ and $\tau_c(j)$ are some values of time specifying, during a selection time T_r, a relative value of quasi-ms voltage decrease caused by distortions of the row and column pulse shapes at the (i,j)-th cell.

Expression (21) represents the proportion to frame frequency of quasi-ms voltage deviation from the static ms voltage value. The values τ_r and τ_c increase with a distance between the cell and the point where driving voltage is applied. Under applying the driving voltage to both ends of a row electrode, maximum value τ_r decreases to one-fourth.

The electrode resistance and capacitance depending on display size.

The values τ_r and τ_c are dependent on shape of front and tail edges of the pulse voltages V_r and V_c formed by voltage sources, on the output resistance of the voltage sources, and on the image patterns. The cell capacitance is dependent on direction of LC molecules, i.e. on ms voltage of the cells.

6). The analysis of the transient process caused by the leading and trailing edges of a unipolar or bipolar pulse (V_r or V_c) at any point of a RC-long line shows that:

- The quasi-ms voltage of LCD cells, which is determined by $\tau_r(j)$ or $\tau_c(i)$ of (21), varies (decreases) at each point of the long line proportionally to the squared amplitude of an input pulse;
- two sharp voltage pulses whose separation at level V_o is wide enough to provide the damping of the transient process ensure the changes of the quasi-ms voltage that is half as much as that caused by a single bipolar pulse symmetric about V_o.

Voltage pulses with stepped edges provide a decrease of $\tau_r(j)$ and $\tau_c(i)$ by a few times. A single step in the leading pulse edge RC/2 wide or over (RC/8 wide for the row electrode powered at both ends) can decrease the change of the quasi-ms voltage of cells by as many as four times. Two such steps allow almost full compensation of the decreased part of quasi-ms voltage change at the leading edges by the increased

part of quasi-ms voltage change at the trailing edge. It is important that this technique provides the suppression of unwanted changes of the cell quasi-ms voltage caused by distorted pulse shapes to the degree almost independent of capacitance C_{ij} of particular cells.

7). Any change of the voltage on a distributed-resistance electrode gives rise to changes in the voltages on cells of crossed capacitance-coupling electrodes (cross-laying, cross-talks). The cross-laying dies down in a recharging time of cell's capacitance C_{ij}. Clear that the cross-laying on column electrodes are caused by voltage changes on row electrodes and vice versa. The distribution of cross-laying over the display electrodes is dependent on the brightness of particular display pixels (display pattern), the order in which driving pulses come to the electrodes, and the amplitude of driving pulses.

Cross-laying on the row electrode can be divided in two types.

The laying of the first type arises on the i-th row electrode during the selection period T_r. This laying brings about the changes of the quasi-ms voltage of the (i,j)-th cell that are determined, to a first approximation, by the difference between the numbers of positive and negative polarity pulses on all column electrodes within period T_r. In this approximation, the quasi-ms voltage of all cells of the selected row undergoes the unwanted change $\pm 2U_{gr}^2 \tau_r \sqrt{A} / \sqrt{N} T_r$ (where A is the display aperture). This change of the quasi-ms voltage can lead to the brightness distortions up to 50% as large as those caused by distorted pulse shapes on the row electrode.

The greatest negative effect on the image quality is caused by laying of the second type. This type of laying occurs on the row electrode at times other than selection period and gives rise to distortions of the quasi-ms voltage of the (i,j)-th cell that can be $\sqrt{N}$ times greater than those attributed to the laying of the first type.

The changes of quasi-ms voltage of LC cells is much affected by the difference in the resistance of output transistors (of microcircuit driver) responsible for charging and discharging of the load capacitance: these transistors set the widths of the leading and trailing edges of the driving pulses. The drivers whose transistors have the same output resistance cause the least cross-laying changes of quasi-ms voltage.

8). Another timing diagrams necessitate the changes of not only voltage levels, but also the design characteristics of the display affecting parameter N_{max}.

Let us assume that, during each row time interval T_r of row one-line or multiple-line selection, the basic customary signal voltages setting brightness of (i,j)-selected pixel (by means of pulse-width modulation or/and of frame modulation) and some added voltage levels decreasing parasitic effects are applied to column electrodes. Each type of the added voltage levels has the identical constant magnitude and identical constant time duration. The first type of the level has t_o-duration and a value equal to a reference voltage V_o called here a zero level as well. The second type consists of two voltage levels having $t_m/2$-duration, the same module V_m, and different polarities relative to V_o. This set of voltage levels is said to by a quasi-zero level having the total t_m-duration. Let us write $k_m = (V_m/V_c)^2$, where V_c is the column voltage value for the correct (in the afore-mentioned sense) one-line addressing having the same t_o- and t_m- durations and the level V_m equal to V_c. Writing and solving the corresponding characteristic equations (not presented here), we obtain that N_{max} of the LCD driven correctly by the said timing diagram must have the value:

$$N_{maxo} = N\frac{1 - t_o/T_r - t_m(1-k_m)/T_r}{(1 - t_o/T_r - t_m/T_r)^2} \qquad (22)$$

If $t_o \ll T_r$, $t_m \ll T_r$, and $k_m = 1$, equality (22) may be written as

$$N_{maxo} \cong N\left[1 + (2t_m + t_o)/T_r\right] \qquad (23)$$

Under considered timing diagram, correct driving the STN LCD having $N_{max}=N_{maxo}$ is possible if all magnitudes of row and column voltages V_{rol} and V_{col} satisfy equalities:

$$V_{rol} = V_{ro}, \qquad (24)$$

$$V_{col} = \frac{V_{co}}{\sqrt{1 - t_o/T_r - t_m(1-k_m)/T_r}} \qquad (25)$$

The values V_{ro} and V_{co} are given in expressions (15) and (16), (17) and (18), (19) and (20) for the various types of addressing.

V_m relates to U_{gr} as

$$V_m = \frac{\sqrt{k_m}\, U_{gr}/\sqrt{2}}{\sqrt{1 - t_o/T_r - t_m(1-k_m)/T_r}} \qquad (26)$$

From this it follows that two-line addressing having, during T_r-selection period, additional level V_o of width t_o and two additional opposite-polarity $t_m/2$-wide levels of equal amplitude $V_m=U_{gr}$ requires the column (signal) voltage V_{col} equal to U_{gr}. The minimal value of N_{max} that is correctly driven by this selecting procedure is governed by the following formula:

$$N_{maxo} = \frac{N}{(1 - 2t_o/T_r)^2} \qquad (27)$$

Let us assume now that in addition to frame selection time NT_r of each frame period T_F, some time interval T_a is added. In this case, there exist the equality $T_F = NT_r + T_a$ instead of the usual equality $T_F = NT_r$. Suppose during the time T_a, the voltage V_o is applied to row electrodes and quasi-zero voltage V_{m1} (that means $\pm V_{m1}$) is applied to column electrodes. Let us write $k_{m1} = (V_{m1}/V_c)^2$, where V_c is the column voltage value for the correct one-line addressing with the same added T_a-duration of the quasi-zero level V_{m1} equal to V_c, and let us write $r=T_a/T_F$. From the corresponding characteristic equations (not presented here), we obtain that N_{max} of the LCD driven correctly by the said timing diagram must have the value N_{maxo}:

$$N_{maxo} = N + k_{m1} r \qquad (28)$$

Under considered timing diagram, correct driving the STN LCD having $N_{max}=N_{maxo}$ is possible if all magnitudes of row and column voltages V_{ro2} and V_{co2} satisfy equalities:

$$V_{ro2} = V_{ro}\sqrt{1 + r/N}\,, \qquad (29)$$

$$V_{co2} = V_{co}\sqrt{\frac{1 + r/N}{1 + k_{m1}\, r/N}} \qquad (30)$$

The values V_{ro} and V_{co} are given in expressions (15) and (16), (17) and (18), (19) and (20) for the various types of addressing.

These results are applicable to the case, when the quasi-zero levels of voltage are applied to electrode on average, when the level of one polarity is added in the first

frame and the level of the other polarity is added in the second frame. These results are useful also to the case, when several (one, two, ...) types of quasi-zero levels having different values V_m are applied to signal electrode in each time interval T_r or on average.

The above schemes of driving can be used in displays with $N_{max} > N_{maxo}$, if the driving voltages for row and column electrodes are governed by relations (11) or (12) in which η is defined as $\eta=\sqrt{1-N_{max\,0}/N_{max}}$ and V_{ro} should be replaced by either V_{ro1}, or V_{ro2}, or V_{ro3} and V_{co} by either V_{co1}, or V_{co2}, or V_{co3}.

The expressions for parameter N_{max} and for row and column voltages allow evaluation of the effect of the voltage-time diagram forms on the imaging quality of the display. This evaluation helps to define conditions necessary for good image quality.

The above theoretical introduction serves to support the feasibility of the driving method described below.

DESCRIPTION OF THE INVENTION

The invention involves a few embodiments each of which improves the image uniformity and contrast of LC displays and increases their operation speed and dimensions. The embodiments allow the characteristics of passive-matrix displays to compare with active-matrix ones.

The first embodiment is the first variant of the method of driving a LCD. The LC display has a panel including substrates having an array of scanning (row) electrodes on one of substrate and an array of signal (column) electrodes on other substrate. A LC material interposed between the both substrates sets LC cells between the said electrodes at their intersection points. LC cell generates display element (or pixel) of the display, sets its size (directly or as the initial element for a projecting display) and defines change its brightness as a function of the voltage on the cell electrode.

Scanning electrodes are selected in one-by-one or group-by-group sequence by applying scanning voltages to the selected scanning electrodes and applying a reference voltage (V_o-level) to the non-selected scanning electrodes. During a selection period T_r, signal (column) electrodes are energized by either voltages

different from reference level V_o (called signified levels), or V_o-level, or combinations of both. These signified and reference voltage levels are called basic levels as different (current) brightness of selected pixels is obtained by varying their combinations or their durations.

Besides, during a selection period T_r an additional V_o-voltage level having a constant duration (t_o) is applied to the signal electrode. It is these to-wide levels of value V_o that make the point of the first variant of the method. This additional level is applied between two levels of opposite polarities (the polarity is determined relative to the level V_o). When there are no signified levels of both polarities within the period T_r, additional voltage is applied to the column electrode either together with the reference voltage if it is present (thus increasing the width of the reference-voltage level) or at any portion of T_r if the reference voltage is absent.

The first variant of the method allows a twofold decrease of the parasitic change of the quasi-ms voltage of LC cells. The first variant of the method results in the improved image uniformity and contrast, and greater screen dimensions and operation speed (the latter is able due to the increased cell-selecting rate).

Applying the additional voltage decreases the portion of interval T_r that is suitable for pulse-width, frame or any other kind of modulation and necessitates the change of display parameters.

Varying the widths of basic voltage levels on the signal electrodes within T_r should follow a particular rule. According to this rule for the case of one-line selection, the total duration of signified-levels is kept constant and equal to $T_r - t_o$ within T_r. When a group of rows is selected simultaneously, a certain mean parameter is maintained constant and equal $T_r - t_o$ relative to every period T_r of the selecting. This parameter is defined as the averaged over period T_r sum of products of durations of every basic signified level to square of inverted ratio of the said signified-level modulus (relative to V_o) to the modulus for correct one-line addressing of the same display. The said one-line addressing is realized with the same constant duration t_o of the said additional V_o-level. The averaging over period T_r is obtained by time-averaging of the said sum during all periods of selection the same display elements in frame time and by multiplication the result into T_r.

Correct driving by this variant of the method requires to design and make the screens having constructive parameter N_{max} to be equal or greater than its minimal value relating to the timing diagram of this variant (N_{maxo}). According to (22), $N_{maxo}=\frac{N}{(1-t_o/T_r)}$. The appropriate amplitudes of driving levels V_{rol} and V_{col} can be defined from (24) and (25). From (25) it follows that correct L row-selection with help of the additional level of width t_o and amplitude V_o involves a $\frac{1}{\sqrt{1-t_o/T_r}}$ times increase of level amplitudes for all signified levels.

The prototype of the variant of the method considered is the method of one-line addressing of a LC display without pulse-length modulation (item 1, US patent 5,157,387 by Seiko Epson; see the fifth prototype). The key feature of that method is generation of two levels of the signal voltage within each selection period.

FIG.10 shows the implementations of the prototype method (see diagrams for V_{cj1}, V_{cj2}, and V_{cj3}), including the implementation that uses reference voltage V_o as one of the two levels.

The prototype method allows reducing of unevenness of display caused by cross-talks.

For one-line addressing, the first variant of the method under consideration differs from the prototype method in that it uses an additional reference voltage V_o which is applied to the signal electrode within period T_r between two signified-level of opposite polarities. In this case during period T_r, depending on the image displayed, three voltage levels, rather than only two can be applied to the signal electrode.

Another difference is multiple-row addressing.

FIG.16 presents time diagrams of voltages V_{ri} and V_{cj} applied to the scanning and signal electrodes in case of one-line addressing as they should be in the first variant of the method considered. Pixels are set to "on", "off", and to intermediate ("gray") states. In the diagram V_{cj}, the cursors mark periods to during which voltage V_o is applied to signal electrodes.

Unlike the diagrams shown in FIG.5 (first prototype method) and all diagrams in FIG.10 (fifth prototype method), these diagrams V_{cj} have additional level V_o applied over interval T_r between two signified-level V_c of opposite polarities. The diagram for V_{cj1} in FIG.10 looks very much like the diagram for V_{cj} in FIG.16 but does not have three voltage levels within T_r.

FIG.17 shows time diagrams of row selecting voltages V_{ri} and $V_{r(i+1)}$ and column signal voltage V_{cj}. The diagrams cover a length of two frame periods and explain the work of the first variant of the method in the two-line addressing mode considered. This addressing can be compared to the eighth prototype method as a variant of multiple-line addressing mode of the method discussed. In the diagram for V_{cj} the cursors mark the periods t_o during which reference voltage V_o is applied. These intervals are absent in the diagrams of the eighth prototype method. Diagram V_{cj} sets the states of simultaneously selected pairs of pixels to (on on), (off off), and (gray gray) with the aid of pulse-length modulation. This technique is absent in the eight prototype method and is introduced by the eleventh variant of the method.

The second embodiment is the second variant of the method of driving a LCD. The LC display is described in the first embodiment.

Scanning electrodes are selected in one-by-one or group-by-group sequence by applying scanning voltages to the selected scanning electrodes and applying a reference voltage V_o to the non-selected scanning electrodes.

During a selection period T_r, signal electrodes are energized by basic voltage levels consisting of either voltages different from V_o (signified), or level V_o, or combinations of both. The basic levels set current values of brightness obtained on a selected pixel or on pixels of a selected group by varying their combinations or their width. A voltage that compensates the unwanted distortion of the cell quasi-ms voltage (which affect the pixel brightness) is also applied to the screen electrodes.

The peculiarity of the second variant of the method is applying, during the selection period, of two additional voltage levels having different polarities, the same constant modules of deviation from V_o-level, and constant and equal durations to the signal electrode. These two additional $t_m/2$-duration V_m-high levels of opposite polarity to reference voltage V_o were called by us the quasi-reference level of t_m-

duration. These levels do not control the current pixel brightness, but set a constant number of voltage switches on a signal electrode over a frame period for any pattern on the screen. The trick allows almost full removal of fluctuations of the cell quasi-ms voltage that is caused by pulse edge distortions. The residual fluctuations that cannot be eliminated this way are determined by the dependence of cell capacitance on the cell quasi-ms voltage and are relatively small. The trick also augments considerably the efficiency of compensating voltages, which are used to decrease the unwanted changes of cell brightness. The examples of particular compensating voltage are given in the seventh and eighth variants of the method. The residual unwanted fluctuations are removed by the ninth variant of the method (see tenth embodiment).

The use of the second variant of the method improves the image uniformity and contrast, and increases the display size and speed of operation.

The prototype of this second variant of the method is the method for activating an LCD (item.31, US patent 5,157,387 by Seiko Epson; see fifth prototype method) that has the following features:

- a selecting voltage is applied to one of the scanning electrodes,
- during period T_r, two-level voltages are applied to the signal electrodes, the voltage of one (high) level being applied for a primary time interval and the voltage of the other (low) level for the secondary time interval,
- the relative duration of the primary and secondary intervals determines the contrast gray level of the pixel.

Use of the prototype method results in the generation of substantially homogeneous cross-talks noise over the entire display.

The second variant of the method differs from the prototype method in that:

- it uses multiple-row selecting as well,
- it uses voltages compensating changes of the cell quasi-ms voltage,
- during period T_r, two additional voltage levels of opposite polarity, the same constant amplitude and constant equal durations are applied to the signal electrode,

- the durations of the opposite-polarity additional levels do not govern the image contrast of the pixel.

In the second variant of the method the portion of period T_r used for pulse-length or frame modulation is decreased to T_r-t_m. In the correct one-line addressing mode, the total width of signified-level is kept constant and equal to T_r-t_m for period T_r. In the correct multiple-row addressing a certain mean parameter is kept constant and equal to T_r-t_m relative to every period T_r of the selecting. This parameter is defined as the averaged over period T_r sum of the products of durations of every basic signified level to square of inverted ratio of the said signified-level modulus (relative to V_o) to the modulus for correct one-line addressing of the same display. The said one-line addressing is realized with the same constant values of duration $t_m/2$ and the same constant V_m-amplitudes of the said pair of additional levels. The averaging over period T_r is obtained by time-averaging the said sum during all periods of selection the same display elements in frame time and by multiplication the result into T_r.

It is sensible to use the first and second variants of the method together. In this case T_r-t_m is replaced by $T_r-t_m-t_o$.

Implementation of the second variant of the method requires N_{max} of the display to be no less than N_{maxo}, which is found from (22) or (23).

Driving voltage amplitudes V_{rol} and V_{col} that ensure correct driving of the display with the value N_{maxo} possible for a presented addressing mode can be determined from (24) and (25).

FIG.18 shows time diagrams of driving voltages V_{ri} and V_{cj} which are applied to the i-th scanning and j-th signal electrodes in accordance with the said variant of the method for case of the one-line addressing. The diagrams cover a length of two frame periods. The cursors in V_{cj} diagram mark additional quasi-reference levels of width $t_m/2$. Here the amplitude of these levels is shown equal to the basic voltage levels, which generally may not be the case. (In tenth embodiment of the invention, for example, the level V_m unequal to the basic voltage can be used for obtain signal voltage pulses of stepped shape front). The cursors also show additional V_o-levels that are introduced in accordance with the first driving variant of the method. Diagram V_{cj} sets particular pixels to "on", "off", and "gray" states.

FIG.19 shows time diagrams of driving voltages V_{ri}, $V_{r(i+1)}$ and V_{cj} which are applied to the i-th and (i+1)-th scanning and j-th signal electrodes in case of the two-line selection for a length of two frames. The diagrams are given to exemplify the use of the second driving method in the multiple-row addressing mode. The additional levels of width $t_m/2$ and opposite polarity that are applied to the signal electrodes are marked with the cursors. The additional levels are shown equal to the basic levels as well. The cursors also mark the additional levels of amplitude V_o and width t_o. Diagram V_{cj} shows states (on, on), (off, off), and (gray, gray) of pixel pairs selected by pulse-length modulation in accordance with the eleventh embodiment of the invention.

This embodiment is the main for the method presented and assists at all other variants of the method.

The third embodiment is the third variant of the method of driving a LCD. The LC display is described in the first embodiment.

Scanning electrodes are selected in one-by-one or group-by-group sequence by applying scanning voltages to the selected scanning electrodes and applying a reference voltage V_o to the non-selected scanning electrodes.

During a selection period T_r, basic-level voltages (either a signified-level, or levels, or reference-level, or combinations of signified- and reference- levels) together with the additional levels of the same constant modules V_m, of constant and equal durations ($t_m/2$) and opposite polarity are applied to the signal electrode. The duration of the basic-level can be varied from a zero duration to a certain value to provide control of brightness of a selected pixel or selected group of pixels.

The new point of the variant of the method consists in a particular order the voltage levels are applied to signal electrodes over period T_r. The order is direct or reverse. The additional levels of deviation V_m of one polarity relative to the basic level Vo allocated to the boundary portions of the period T_r (one level is allocated to the beginning portion and the other level is allocated to the end portion of T_r).

In succeeding periods T_r, the said orders of applying the voltage levels to the signal electrode alternate on the basis of changing of the polarity of the voltage deviation the level from V_o-level in the beginning (accordingly, in the end) of the

period T_r. The positive polarity is set in the beginning of one period T_r and the negative polarity is set in the beginning of the next period T_r. The trick allows the end signified-level in one period T_r to merge with the beginning level in the next period T_r.

Such alternation is gone on in the course of some alternating time. The number of periods T_r over which these polarity alterations occur can be limited by the additional time during which the compensation voltage is applied to the screen electrodes (see, for example, the eighth embodiment). It is possible a different order the levels applied to the signal electrodes (see the fifth embodiment) or change of the reference voltage level under one-line addressing (see FIG.18), etc.

The joint use of the third, second, and first variants of the method for driving a LCD screen is demonstrated in FIG.18 (one-line addressing mode) and FIG.19 (two-line addressing mode). The diagrams for V_{cj} in the two figures illustrate the alteration of voltage polarity, including the additional levels in the beginning and the end of period T_r (positive-negative, negative-positive, etc.). The number of voltage changes and the parasitic change of the quasi-ms voltage of LCD cells decreases twofold.

The prototype for the third variant of the method is the US patent 5,162,932 by Matsushita (the third prototype method), the patent-prototype aimed at increasing the image quality across the screen.

FIG.8 shows the timing diagrams of the row and column voltages corresponding to the prototype.

The features of the prototypes are:

- one-line addressing mode;
- during the scanning period T_s (where $NT_s=T_F$ and N is the number of rows being scanned, T_F is the frame period) two levels, V_{on} and V_{off}, are applied to the signal electrode for illuminating and disilluminating the selected pixel;
- the row selection period T_r is less than scanning period T_s;
- the allocation V_{on} and V_{off} to a beginning and to an end portions of the scanning period T_s is reversed at intervals of succeeding scanning periods.

The variant of the method proposed differs from the prototype method in the following points:

- there is no sign of the row selection period T_r being less than the scanning period T_s;
- more than two voltage levels are applied to a column over period T_r ;
- there is a multiple-row addressing as well;
- during period T_r, two additional levels of equal amplitude, width, and opposite polarity (about the reference level V_o) are applied to a signal electrode;
- these additional levels goes in the beginning and end of period T_r;
- during T_r, all voltage levels are applied in a certain order to a signal electrode;
- the sign of alternation at intervals of succeeding scanning periods is the alternation of polarity (positive-negative, negative-positive) rather than the alternation of the state "on"-"off", "off"-"on".

The amplitude of the row selecting level in the variant of the method considered is less than that in the prototype method. This decreases the frame response effect.

The use of the third variant of the method improves the image uniformity and contrast, and makes it possible to increase the display size and operation speed.

The forth embodiment is the forth variant of the method of driving a LCD. The LC display is described in the first embodiment.

Scanning electrodes are selected in one-by-one or group-by-group sequence by applying scanning voltages to the selected scanning electrodes and applying a reference voltage V_o to the non-selected scanning electrodes.

During a selection period T_r, basic-level voltages (either a single or a few signified levels, or reference level, or combinations of signified and reference levels) together with the additional levels of the same constant modulus (V_m) of deviation from V_o-level, opposite polarities, and constant and equal durations ($t_m/2$) are applied to a signal electrode. The duration of the basic-level can be varied from a zero duration to a certain value to provide control of brightness of a selected pixel or a selected group of pixels.

Driving levels are applied, during the period T_r, to the signal electrode in a specific order, in direct one or in reverse one. The additional level Vm of one polarity

is allocated to the beginning portion of the period T_r and of the opposite polarity is allocated to the end portion of the period T_r.

The new point of the variant of the method is that levels of opposite polarity (relative to V_o) are applied to the column electrodes in order providing spatial compensation of cross-talk laying. For that voltage levels applying, during the period T_r, to adjacent signal electrodes or to signal electrodes located one or two electrodes further or to signal electrodes having another type of activation sequence so that the levels allocated to the beginning portion (and, accordingly, to the end portion) of the period T_r have deviations of opposite polarities from V_o-level.

An example of joint use of the forth, third, second and first LCD driving variants of the method for the two-line addressing is given in FIG.20. The figure shows the timing diagrams of row-driving voltages V_{ri} and $V_{r(i+1)}$ and column-driving voltages V_{cj} and $V_{c(j+1)}$, and the resultant voltage ($V_{cj}-V_{ri}$) at the (i,j) cell. The diagrams cover two fields of one frame and the beginning of the first field of the next frame. The diagrams describe the instance when all display cells have the same brightness, viz., they are all in the "on" state. Without using the variant of the method, the image would have had the highest possible level of cross-talk laying and largest shadowing of white pixels in this case. Small dark areas against the white background would have had maximal whiteness and the image would have had the lowest contrast. FIG.20 shows row voltage spikes (cross-talk laying of first and second type) caused by synchronous changes in column voltages.

It follows from FIG.20 that opposite polarities of the driving voltage on neighboring signal electrodes result in opposite polarities of the first-type cross-talk laying on selected row electrodes and compensation of variations of the quasi-ms voltage of corresponding cells. The best compensation is achieved by employing driving electronics whose work relies on the seventh embodiment (this design provides the least joint effect of opposite-polarity voltage spikes on the cell quasi-ms voltage by making their amplitudes almost equal).

The forth variant of the method also provides an over two times decrease of the oscillations of the cell quasi-ms voltage caused by cross-talk laying of the second type (this type of laying arises in the period between successive row selection pulses and can bring about the greatest oscillations of the cell quasi-ms voltage). The effect is achieved by separating in time, within period T_r, the moments at which the driving voltages across the neighboring signal electrodes (carrying pixels of the same brightness) change. FIG.20 illustrates a particular case when the opposite-polarity laying spikes of the second type are separated in the first field of the frame and compensated almost fully in the second. In this particular case and some other instances, the technique allows as many as fourfold decrease of the effect of the row laying of the second type on the cell quasi-ms voltage. There are uniform-brightness images (e.g. a gray image with the cell quasi-ms voltage of U_{gr}^2) for which the use of the variant of the method considered can reduce the cell quasi-ms voltage variations caused by cross-talks of the second type almost to zero.

The prototype of the variant of the method is the US patent 5,162,932 (the third prototype method) by Matsushita in which the one-line addressing mode is used. Within each period Tr a signal electrode receives two voltage levels, "on" and "off", one of the two (either "on" or "off") going in the beginning of period T_r, the other in the end, and the both exchanging places with each successive T_r.

The variant of the method presented differs from the prototype in the first six points stated in the description of the distinction of the third variant of the method from its prototype and in the point consisting in feeding the neighboring, or alternate signal electrodes, or particular number electrodes further with pulses that have opposite polarity relative to V_o and go either in the beginning or at the end of the period Tr.

The use of the fourth variant of the method improves the image uniformity and contrast, and makes it possible to increase the display size and operation speed.

The fifth embodiment is the fifth variant of the method of driving a LCD. The LC display is described in the first embodiment.

Scanning electrodes are selected in one-by-one or group-by-group sequence by applying scanning voltages to the selected scanning electrodes and applying a reference voltage V_o to the non-selected scanning electrodes.

During a selection period T_r, basic-level voltages (either a single or a few signified levels, or reference level, or combinations of signified and reference levels) together with the additional levels of the same constant modulus (V_m) of deviation from V_o-level, opposite polarities, and constant and equal durations ($t_m/2$) are applied to a signal electrode. The duration of the basic-level can be varied from a zero duration to a certain value to provide control of brightness of a selected pixel or a selected group of pixels.

Driving levels are applied, during the period T_r, to the signal electrode in a specific order, in direct one or in reverse one. The additional level V_m of one polarity about V_o-level is allocated to the beginning portion of the period T_r and of the opposite polarity is allocated to the end portion of the period T_r.

The variant of the method provides compensation of cross-laying in course of time. For this purpose, the order in which the voltage levels are applied to the signal electrode within periods T_r is alternated in T_r-periods of selection the same scanning electrode or the same group of scanning electrodes where the scanning voltages or the scanning voltage groups have identical or opposite polarities about V_o-level. The alternation is set in succeeding frame time periods or in a frame time or in two frame times or in accord with other order of comparison in course of time. The rule of the alternation sets alternately the same and opposite directions of the deviation (from V_o-level) of the signal voltage level allocated to the beginning (and, accordingly, to the end) portion of the period T_r and of the deviation (from V_o-level) of the voltage V_r applied to the same selected scanning electrode or to the same selected scanning electrode of the selected group.

The point of the variant of the method consists in that the contributions of cross-talks of the first and second types to the cell quasi-ms voltage cancel out with time because of opposite polarities they have in consecutive frames. Similarly, the variant of the method removes the laying induced on signal electrodes by voltage changes on row electrodes.

An example of joint use of the fifth, forth, third, second and first LCD driving variants of the method in case of two-line addressing is given in FIG.20.

FIG.20 shows the above said alternation of the signal levels within an intervals T_r setting by the second type of successions of voltages V_{cj} and $V_{c(j+1)}$ in the first field of the second frame as compared to the first type of succession of these levels within corresponding intervals T_r in the first field of the first frame, the alternation depending on whether the leading signified level in the period T_r and voltage V_r on a selected row electrode have the same polarity or not. Voltage spikes from signal voltage switches increase the $\frac{1}{T_r}\int_0^{T_r} V_{fi}^2(t)dt$-component of the cell quasi-ms voltage during one frame and decrease it during the other, allowing the fluctuations of the cell quasi-ms voltage to cancel out.

The prototype of the variant of the method is the US patent 5,162,932 (the third prototype method) by Matsushita in which the one-line addressing mode is used. Within each selection period T_r, a signal electrode is fed with two voltage levels, "on" and "off", one of the two (either "on" or "off") going in the beginning of period T_r, the other in the end, and the both exchanging places with each successive T_r (FIG.8).

The fifth variant of the method differs from the prototype in the first six points stated in the distinction of the third variant of the method from its prototype. Additional difference consists in choosing the order of applying signified levels to a signal electrode during period T_r in either succeeding frames, or alternate, or other specifically chosen frames according to whether or not the leading signified level in the period T_r and voltage V_r on a selected row or a particular row of a selected row group have the same polarity relative to V_o.

Levels "on" and "off" exchanging their positions in the beginning and at the end of successive intervals T_r offered in the prototype does not provide the alternating polarity of laying spikes of the same type at particular cells in the neighboring frames and does not compensate the fluctuations of the cell quasi-ms voltage caused by these laying spikes.

When used in combination, the fifth variant of the method augments the effect of the forth variant of the method by removing residual incompleteness of canceling

of the cell quasi-ms voltage variations caused by cross-talks. The forth variant of the method complements, in turn, the fifth by removing residual incompleteness of canceling of the cell quasi-ms voltage oscillation caused by compensation delays over the frame time.

The use of the seventh embodiment augments the effect of the fifth variant of the method.

The use of this variant of the method decreases fluctuations of the cell quasi-ms voltage, improves the image uniformity and contrast, and makes it possible to increase the display size and operation speed.

The sixth embodiment is the sixth variant of the method of driving a LCD. The LC display is described in the first embodiment.

Scanning electrodes are selected in one-by-one or group-by-group sequence by applying scanning voltages to the selected scanning electrodes and applying a reference voltage V_o to the non-selected scanning electrodes.

During a selection period T_r, pulses of voltage are applied to the signal electrode. The pulses set basic-level voltages (either a single or a few signified-levels, or reference-level, or combinations of signified- and reference- levels) together with the additional levels of the same constant modulus (V_m), opposite polarities, and constant and equal durations ($t_m/2$). The duration of the basic-levels can be varied from a zero duration to a certain value to provide control of brightness of a selected pixel or selected group of pixels.

Driving levels are applied, during the period T_r, to the signal electrode in a specific order, in direct one or in reverse one. The additional level V_m of one polarity about V_o-level is allocated to the beginning portion of the period T_r and of the opposite polarity is allocated to the end portion of the period T_r. The order in which the levels are applied to signal electrodes over period T_r is alternated in succeeding periods T_r.

The peculiarity of the variant of the method is that the voltage pulses applied to signal electrodes are split into a number of groups being related to different electrodes and shifted in time concerning their nominal positions in the period T_r. The values of shifting time are set the same for the pulses of a single group, but different

for the pulses of different groups, and constant for certain period (e.g. for a fraction of a field, or a whole field, or a whole frame, or two frames, etc.). After termination the said time period, other values of shifting time are set in certain or in all groups of voltage pulses or other aggregate of groups of voltage pulses is formed with different values of shifting time in various groups, and the said other values of shifting time are set constant for the next time period. After termination the next time period the said process of either changing or setting constant values of shifting time are continued providing zero average deviation of duration of each said additional level from its nominal duration. The shifting time should not exceed $t_m/2$ and may be either positive, or negative, or zero.

The signal voltages switching at different current moments result in voltage spikes on the cell having low amplitudes and opposite polarity and canceling out.

However, signal electrode groups having random time shifts of the driving pulses may give rise to non-uniform suppression of cross-talks. To suppress cross-talks most effectively, the shifting times of voltage pulses in groups should be changed according to the particular rule. Namely after termination of the time period during which the shifting time values of groups of voltage pulses are kept constant, the latest shifting time value is set in the group of pulses, each having the earliest shifting time value, the previous shifting time value is set in the group of pulses, each having the next after the earliest shifting time value, and such changing of shifting time values is applied in other groups up to group of pulses, each having the earliest shifting time value, which are changed to the latest shifting time value.

With K equal-size groups of signal electrodes, the above rule of pulse shift change allows an either 2K-times or K-times decrease in the cell quasi-ms fluctuations caused by the second-type cross-talks subject to whether the first LCD driving variant of the method is used or not used, respectively.

This effect is most noticeable for large enough areas of equally bright cells. To decrease these fluctuations in small display areas of uniform brightness, the pulses that make up a pulse group of the same shift should belong to the signal electrodes that have large enough separation and/or the group should change its composition time to time.

FIG.21 shows three pulse groups V_{c1}, V_{c2}, and V_{c3} applying to three groups of signal electrodes for two frame-length periods of constant pulse shifts. The row selection pulses are not shown. For simplicity sake, the one-line addressing mode is illustrated. The basic voltage levels set the appropriate cell to the "on" state. Selection period T_r has two additional portions of tm/2 wide each for "off" and "on" values. The pulse widths are shown out of scale. A possible change of the pulse polarity from one frame to the other is not shown. The alternation of the voltage levels in going from the period $T_r(n)$ of selecting n-th row to period $T_r(n+1)$ of selecting (n+1)-th row is shown. Two pulse groups V_{c1} and V_{c2} have different time shifts t_1 and t_2 of the opposite directions relative to their original (non-shifted) positions. The third pulse group V_{c3} is not shifted. Diagram V_{ri} shows cross-talks spikes on the i-th row when it is not selected. Diagrams (V_{cj}–V_{ri}) show the resulting voltages of the three display cells, indices (c1, c2, c3) attributing the cells of the i-th non-selected row to the appropriate group of signal electrodes.

Determined as the mean number of induced spikes (their polarity relative to that of the driving pulse must be taken into account), the effect of cross-talks on the cell quasi-ms voltage in each of the three cell groups decreases threefold, to a single cross-talks spike of the three possible within period T_r on average.

Another example is shown in FIG.22. Groups of driving pulses V_{c1}, V_{c2}, and V_{c3} for signal electrodes are not shown in the figure directly. Diagrams (V_{cj}–V_{ri}) for the display cells can determine them by analogy with FIG.21. In contrast to FIG.21, multiple shifts (t_d or $2t_d$) of the same direction are used in FIG.22. Though two shift change periods are enough to decrease the cross-talks effect, maintaining the average width of additional pulses equal to $t_m/2$ requires the order of the pulses within the selection period $T_r(n)$ of the n-th row to change in the following frame as, for example, in the fifth driving variant of the method. As a result, the complete cycle of shift changes grows to four periods of constant in time shifts. Other rules for changing pulse shifts are possible, e.g. succession of combinations of four reference periods shown in FIG.22.

To driving large display areas of constant brightness, all prototype methods, including the US patent 5,162,932 by Matsushita (the third prototype method, which

is most similar to the variant of the method considered), use the driving voltages that bring about considerable cross-talks of the second-type and poor color rendering at high frame rates. The papers presented by researchers from Sharp and Hitachi at SID Symposium in Toronto in September, 1997 (SID'97, pp. M75-M87) consider the techniques that make it possible to decrease vertical and horizontal shadowing caused by cross-talks of different types. That techniques do not use pulse shifts and their efficiency, especially with use of pulse-length modulation, is not high.

Besides removing shadowing effects, the variant of the method considered improves the image uniformity and contrast, makes it possible to increase the display size and operation speed, and allows perfect color rendering.

The seventh embodiment is the device of driving a LC display.

The LC display has a panel including substrates having an array of scanning (row) electrodes on one of substrate and an array of signal (column) electrodes on other substrate. A LC material interposed between the both substrates sets LC cells between the said electrodes at their intersection points. LC cell generates display element of the display and defines change its brightness as a function of the voltage on the cell electrodes. Scanning electrodes are selected in one-by-one or group-by-group sequence by applying scanning voltages to the selected scanning electrodes and applying a reference voltage V_o to the non-selected scanning electrodes. Signal voltages are applied to a signal electrode to set brightness of a selected pixel or selected group of pixels. The display is driven in accordance with the variants of the method presented.

The device of driving a LC display comprises a bunch of row and column drivers (voltage pulsers, VP) and a voltage level generator (VLG, a power supply unit) which feeds other units or blocks and sets levels for row and column pulses. The VP incorporates a block setting timing voltage levels to an output electrode (for short, timing block, TB) that comprises a logic block (LB) and a voltage converter block (VCB) electrically coupled to the LB, and an output transistor block (OTB) electrically coupled to the VCB. The output lead of the OTB is coupled to the display electrode. The LBs for row electrodes are connected by one bi-directional shift register and LBs for column electrodes are connected by the other. All blocks are

electrically coupled to the VLG. The VP for column electrodes may not have a VCB when the display operates, for example, in the two-line addressing mode, in this case the LB is coupled to the OTB directly. The LB input leads are applied with clock and control pulses. The LB for column electrodes is also fed with data signals from a data processing unit.

The peculiarity of the device is an OTB design which sets identical shapes of the voltage spikes of both polarities. The result is better cross-talks compensation for any driving variant of the method used (the best for the fourth, fifth, and sixth variants of the method) and, therefore, the improved image quality (uniformity and contrast), and possibility to grow the display operation speed and dimensions.

FIG.23 shows a block diagram of LC panel 4 driving device. It consists of voltage level generator 1 feeding other blocks and of row and column voltage pulsers 2 and 3. The device generates control pulses enabling the LCD to operate in any row selection mode of presented invention including one-line, two-line or multiple-line addressing.

Voltage pulser 2 has many channels for driving display electrodes Y_1, Y_2,..., Y_i,..., Y_N, while driver 3 has many channels for driving display electrodes X_1, X_2,..., X_i,..., X_N. Each channel of driver 2, e.g. i-th channel, incorporates logic block 5 (LB_i) that sets moments of applying selecting pulses to channel Y_i, voltage converter block 6 (VCB_i), and output transistor block 7 (OTB_i). Block 5 is coupled to block 6, block 6 to block 7, and block 7 to display electrode Y_i. Each channel of driver 3, e.g. j-th channel, incorporates logic block 8 (LB_j) that processes data signals and sets moments of applying signal levels to channel Xj and output circuit block 9 (OTB_j) that is coupled to block 8 and electrode X_j. Input leads 10 and 11 of blocks 5 and 8 are fed with clock and control pulses, leads 12 of block 8 with data signals. Block 5 is coupled to LB_{i-1} and LB_{i+1} and block 8 to LB_{j-1} and LB_{j+1} of the neighboring channels each by own bi-directional shift register whose trigger stages are incorporated in appropriate logic blocks.

Logic blocks 5 and 8 generate low-level voltages whose timing diagrams provide the formation of driving voltages in blocks 6, 7 and 9.

Voltage generator 1 produces at least five voltage levels V_o, V_1, V_2, V_3, and V_4, the levels being measured from a certain common level. Reference level V_o goes to voltage pulsers 2 and 3, levels V_1 and V_4 go to row voltage pulser 2, levels V_2 and V_3 to column voltage pulser 3. Being so that $|V_1-V_o|=|V_4-V_o|$ and $|V_2-V_o|=|V_3-V_o|$, the voltage levels in combination with timing diagrams corresponding to the driving variant of the method must allow LC cells to have the quasi-ms voltages that lies within the working range of the dynamic square voltage – optic behavior of cells (solid line in FIG.15). The dynamic square voltage - optic behavior determines dynamic N_{max} and dynamic contrast, which accounts for image quality.

One of the column voltage levels, e.g. V_2, can be applied to block 2 for supplying blocks 5 and 6 by low-level voltage.

A possible design of block 7 is shown in Fig.24. Signals from the VCB_i set the moments of applying voltages V_o, V_1, or V_4 to the output electrode. The design of block 9 is similar to that of block 7. The difference is replacement of V_1 by V_2 and V_4 by V_3.

Spikes of both polarity caused by cross-talks have identical shapes due to the transistors incorporated in the OTB (e.g. 13, 14, 15, and 16 in FIG.24) that provides the same output resistances for different voltage values, or the deviation not exceeding 10%. Such characteristic of the output transistors results from chosen relations between transistor structural elements (the length and width of the transistor channel, the thickness of the gate oxide, etc.).

There may be difficulties in making transistors of different types with characteristics providing close values of resistance. To avoid these difficulties and to improve cross-talks suppression, another OTB construction incorporates additional transistors (17, 18, 19, and 20 in FIG.25). Transistors 17 and 18 are introduced to make their common with transistor 13 output resistance equal to the output resistance of transistor 14, which was originally somewhat less than the resistance of transistor 13. Having a common output resistance with transistor 15, transistors 19 and 20 are introduced to make the said resistance equal to the output resistance of transistor 16, which was originally somewhat less than the resistance of transistor 15. Additional leads 21 and 22 are common for all blocks 7 (for blocks 9) of the driving system.

After the tailoring of conductivity of transistors 17 and 19 by choosing appropriate voltages across leads 21 and 22, they are left in the on state. This way the output resistances are maintained equal for all voltages applied to the output lead (in all channels).

The function of block 9 is similar to that of block 7 (FIG.25) except that voltage V_1 is replaced by V_2 and V_4 by V_3.

The prototype of the variant of the method considered is the display driving devices presented in the patents for the prototype methods and incorporating output transistors that are electrically coupled to the output leads. However, they do not provide for the output resistances of transistors through which a particular voltage is applied to the output lead to have the same or near values, with deviation not exceeding 10%.

The eighth embodiment is the seventh variant of the method of driving a LCD. The LC display is described in the first embodiment.

Scanning electrodes are selected in one-by-one or group-by-group sequence by applying pulses of scanning voltages to the selected scanning electrodes and applying a reference voltage V_o to the non-selected scanning electrodes.

The signal electrodes are driven by pulses of voltage. The pulses set basic-level voltages (either a single or a few signified-levels, or reference-level, or combinations of signified- and reference- levels) that provide the nominal current values of the cell mean-square voltage and additional levels of the same constant modulus (V_m), opposite polarities, and constant and equal durations ($t_m/2$). The additional levels set a nearly image-independent component of the cell quasi-ms voltage fluctuations that are caused by distortion of column-driving pulses as they propagate down long electrode. Usually negative in polarity, this component grows in amplitude with the increasing distance from the point where the driving voltage pulses are applied to a column electrode. Similar cell quasi-ms voltage fluctuations caused by distortion of row-driving pulses are almost independent of the image pattern, either. Therefore change of brightness of any image pixel from the nominal value caused by these pulse distortions is largely dependent on the pixel location.

The variant of the method is distinguishable in that addition compensation voltages $V_{com}(i)$ are generated for i-row electrodes starting from a particular one and/or addition compensation voltages $V_{com}(j)$ are generated for j-column electrodes starting from another particular one. The amplitudes $V_{com}(i)$ of compensation voltages or durations of them are determined for each row electrode experimentally or analytically (for given timing diagram and frame frequency) to provide best compensation of the cell quasi-ms voltage fluctuations caused by the propagation distortion of column pulses. Similarly, the amplitudes $V_{com}(j)$ of compensation voltages or durations of them are determined for each column electrode experimentally or analytically (for given timing diagram and frame frequency) to provide best compensation of the cell quasi-ms voltage fluctuations caused by the propagation distortion of row pulses. One or several time intervals of duration t_c are added to N selection periods T_r over the frame period. Every compensation voltage $V_{com}(i)$ is applied to i-row electrode during a fraction of, or one, or several t_c-intervals. The compensation voltage $V_{com}(j)$ is applied to j-column electrode during a fraction of, or one, or several other t_c-intervals. The column and row electrodes to which voltages $V_{com}(i)$ and $V_{com}(j)$ are not applied, during t_c-interval, are powered with reference voltage V_o. Instead of voltage V_o, it is possible to use quasi-reference voltage or quasi-reference voltage on average, or their combinations, including combinations with voltage V_o.

The point of the variant of the method is constant (in course of time) value or shape of compensation voltage for particular electrode and a wide range of the cell quasi-ms voltage fluctuations that can be compensated.

The example of timing diagrams for row pulses corresponding to the variant of the method considered is shown in FIG.26. Selection pulses V_r are applied to the first, i-th, (i+m)-th and N-th row electrodes over two frames under a one-line addressing mode and over two fields under a two-line addressing mode. Compensation voltages δV_i, δV_{i+m}, and δV_N of different amplitudes are applied to all row electrodes shown (except the first one) each at the same time. At that time, all column electrodes, including the j-th column, are energized by reference voltage V_o.

The examples (variants) when the row compensation voltages have equal amplitudes and different durations and the examples when the compensation voltages are applied to column electrodes for other time intervals t_c are not illustrated in FIG.26, but can be considered (synthesized) in a similar manner.

The amplitudes of driving voltages V_{ro2} and V_{co2} that provide the correct driving the display having the smallest possible value of $N_{max}=N_{maxo}$ for the given addressing mode can be derived from (28), (29), and (30). N_{maxo} can be found from (31).

The prototype of the variant of the method is the method of driving a passive matrix LC display described in the US patent 5,151,690 by Seiko Epson (the fourth variant) stating the following features in the first item of the patent formula:

- one-line addressing mode is used;

- in addition to the time interval during which the driving voltages are applied to the display electrodes ("the driving times"), there is a period of time ("the compensation time") during which at least partial compensation of the image distortions appeared in the earlier period takes place;

-during the period of compensating time, selection pulses are not applied to row electrodes, and one or more signal electrodes are energized by an additional voltage necessary for at least partial compensation of distortions caused by changes of image in the earlier period.

To implement this technique, the second item of the patent formula suggests that the compensation voltage should be set in accordance with the number of variations between "on" and "off" states on a particular column electrode for the previous period of a time preceding the compensating time.

The row and column voltage diagrams corresponding to the prototype method are shown in FIG.9. Voltage V_{ri} is applied to row Y_i, voltage V_{cj} to column X_j, V_{ij} is the voltage of the (i,j)-th cell. V_{o1} and V_{o2} are reference voltages in the neighboring frames. After all row electrodes are selected, the compensation voltage is applied to column X_j for the time t_c whose length is dependent on the number of voltage changes on electrode X_j during the previous period.

The variant of the method considered differs from the prototype method in the following points:

- multiple-row selection mode is possible;

- the effect that the propagation distortion of pulse shapes has an impact on the cell quasi-ms voltage is made image-independent by using certain tricks, e.g. by applying quasi-reference voltages to signal electrodes;

- voltage $V_{com}(i)$ is applied to the i-th row electrode to compensate the effect of column pulse propagation distortions;

- there is no relation between the parameters of compensation voltages $V_{com}(i)$, $V_{com}(j)$ and the brightness distribution across the display in the previous period of time.

The seventh variant of the method improves the image uniformity and contrast, makes it possible to increase the display dimensions and operation speed.

The ninth embodiment is the eighth variant of the method of driving a LCD. The LC display is described in the first embodiment.

Scanning electrodes are selected in one-by-one or group-by-group sequence by applying scanning voltages to the selected scanning electrodes and applying a reference voltage V_o to the non-selected scanning electrodes.

The signal electrodes are driven by pulses of voltage. The pulses set basic-level voltages (either a single or a few signified-levels, or reference-level, or combinations of signified- and reference- levels) that provide the nominal current values of the cell mean-square voltage and additional levels of the same constant modulus (V_m), opposite polarities about V_o, and constant and equal durations ($t_m/2$).

The additional levels set a nearly image-independent component of the cell quasi-ms voltage fluctuations that are caused by distortion of column-driving pulses as they propagate down long electrode. This component grows in amplitude with the increasing distance from the point where the driving voltage pulses are applied to a column electrode. Change of brightness of any pixel from the nominal value caused by these pulse distortions is dependent on the pixel location.

The variant of the method is distinguishable in that a row compensation voltage $V_{com}(i)$ is generated starting from a particular row. The amplitudes $V_{com}(i)$ of

compensation voltages or/and their durations are determined for each row electrode experimentally or analytically (for given timing diagram and frame frequency). The compensation voltage $V_{com}(i)$ is added to (superimposed on) the scanning voltage applying to the i-row electrode at a particular moment within the row selection period to provide compensation of the decreased quasi-ms voltages of cells of the i-th row caused by the propagation distortion of column-driving pulses.

The example of the timing diagrams of the row voltage corresponding to the variant of the method is shown in FIG.27. Selection pulses V_r are applied to the first, i-th, (i+m)-th and N-th row electrodes for the period of two frames (under a one-line addressing) or two fields (under a two-line addressing), added compensation pulses V_i, V_{i+m}, V_N of different amplitudes being shown by a dotted line. V_{cj} illustrates the timing diagrams of driving voltages for the j-th signal electrodes.

The prototype of the variant of the method considered is the method of driving a passive matrix LC display given in the US patent 5,151,690 by Seiko Epson (the forth prototype method).

In addition to the points in which the seventh variant of the method differs from the forth prototype method, the eighth variant of the method does not have the prototype's distinguishing point of using a separate time interval during which the compensation voltage is applied to the signal electrodes.

The distinguishing point of the variant of the method is use of constant (in course of time) values of the compensation voltage for each row electrode and a wide range of the cell quasi-ms voltage fluctuations that can be compensated. There is also no need in allocating separate compensation intervals of duration t_c within the frame period and in increasing N_{max} of the display.

The eighth variant of the method improves the image uniformity and contrast, makes it possible to increase the display dimensions and operation speed.

The tenth embodiment is the ninth variant of the method of driving a LCD. The LC display is described in the first embodiment.

Scanning electrodes are selected in one-by-one or group-by-group sequence by applying pulses of scanning voltages to the selected scanning electrodes and applying a reference voltage V_o to the non-selected scanning electrodes. The pulses to signal

electrode set basic levels (either a single or a few signified-levels, or reference-level, or combinations of signified- and reference- levels) that provide the nominal current values of the cell mean-square voltage.

However, shape degradation of driving pulses as they propagate down a long line electrodes results in unwanted changes of the quasi-ms voltage of the cells and poorer optical performance of the pixels. The values of change are a function of cell capacitance dependent on the current value of quasi-ms voltage being varied. So far the known techniques could not cope with the negative effects related to cell capacity variations dependent on display pattern.

The ninth variant of the method is designed to eliminate the effect of pulse shape distortion caused by propagation of pulses down long electrodes on quasi-ms voltage of cells and to suppress the effect of shadowing caused by variations of the cell capacitance.

The distinctive point of the variant of the method consists in a special pulse shape. The pulse shape provides on the one hand the necessary values of the quasi-ms voltage at the cells of a long electrode and on the other hand self-compensation of the quasi-ms voltage changes caused by distortions of the pulse edges as the pulses propagate down the electrode, including the electrode with non-linear properties. The leading and trailing edges (fronts and tails) of a pulse are considered here as a voltage jump up from and down to the reference voltage V_o.

The transient process accompanying voltage pulse on a long electrode can be approximated with an exponent, the transient time being dependent on the position (i,j) of a particular cell. As the leading and trailing edges have the same transient times, driving pulse with stepped leading edge can provide the decrease in the cell quasi-ms voltage that is equal or nearly equal to the increase in this value caused by the trailing edge. To ensure self-compensation of the cell quasi-ms voltage fluctuations, the profile of the leading edge should provide the decrease of cell quasi-ms voltage three times less than that caused by the pulse with steep leading edge.

The examples of timing diagrams of driving pulses with stepped leading edges that suffered distortion from propagation are shown in FIG.28. The leading and trailing edges of different polarity relative to the level V_o are shown. Pulse V_1 can

decrease the cell quasi-ms voltage fluctuations fourfold as compared to that related to conventional rectangular pulses. Having two steps in the leading edge, pulse V_2 can cancel the cell quasi-ms voltage fluctuations if the step tops are long enough to provide sufficient dying of the transient processes in the long electrode.

The front having stepped shape can be formed by other ways. One of the ways is to apply, in each T_r-period, two or three additional quasi-reference levels on average to the signal electrode, the said levels having the same constant durations ($t_m/2$) and different values of module (V_{m1} V_{m2}, ...).

The joint use of the ninth and fifth variants of the method decreases or eliminates the cell quasi-ms voltage fluctuations caused by the dissimilarity of voltages of opposite electrode at the times of arrival of the pulse edges at one of the electrode.

The method described in the US patent 5,301,047 by Hitachi (the second prototype method) is most close to the variant of the method considered. The prototype method uses the one-line addressing mode as in the first prototype method, high-frequency voltages of various forms being added continuously to either the row, or column, or row and column voltage levels. The aim of the prototype method is to improve the uniformity of the image displayed. FIG.7 gives the voltage profile at the ij-th cell produced by adding continuously chopping wave to row and column driving voltages.

The ninth variant of the method differs from the second prototype method in the following points:

- driving voltages are not superimposed continuously with high-frequency pulses of any shape;

-stepped or nearly stepped leading edge of the driving pulses for display electrode provides self-compensation of the pulse distortion effect on the cell quasi-ms voltages.

The ninth variant of the method improves the image uniformity and contrast, makes it possible to increase the display dimensions and operation speed.

The eleventh embodiment is the tenth variant of the method of driving a LCD. The LC display is described in the first embodiment.

Scanning electrodes are selected in two-by-two sequence, at least twice over the frame period. The polarities of scanning voltages (V_{r1} and V_{r2}) alternates according to a particular rule, e.g. the voltages have the same polarity (relative to level V_o) in the first field and opposite polarity in the second one. It is possible to use other rules providing the said alternation on average. The row electrodes not being selected carry the reference voltage V_o.

During a selection period T_r, basic-level voltages together with additional levels are applied to a signal electrode.

The distinguishable point of the variant of the method is that two components of the signified levels, called informational and quasi-reference equalizing, are applied to the signal electrodes to provide the pulse-length modulation of selected cells instead of the frame modulation used in the multiple-line addressing mode.

Depending on the brightness a_{ij} and $a_{(i+1)j}$ of the pixels located at the intersection of i-th and (i+1)-th row electrodes and j-th column (a_{ij} and $a_{(i+1)j}$ may vary from –1 to +1, for example), the column receives the informational-level whose duration is proportional to and polarity is the same as that of the half sum of the brightness values $(a_{ij}+a_{(i+1)j})/2$ under the row-selection pulses of the same polarity, or the half difference $(a_{ij}-a_{(i+1)j})/2$ under the row-selection pulses of opposite polarity. The duration of informational-level can be corrected for the non-linear electro-optic behavior of the LC display element.

The informational level can be as wide as, or shorter than period T_r. For example, if in accordance with the first and second variants of the method, additional voltage levels are applied to the signal electrodes in addition to the informational-level, the maximal duration of the informational-level is set equal to $T_r-t_m-t_o$.

It is clear that the total duration of the informational levels can vary for the time of two selection periods.To keep the total duration of all signified levels related to the given pixels constant, the quasi-reference equalizing levels of variable duration and amplitude equal to that of the informational level is used. In the absence of the additional levels, the amplitude of the column-driving pulses relative to V_o is defined from (18). Otherwise, the amplitude is found using (25). The total duration of all informational and equalizing levels over two periods T_r is equal to or greater than the

maximal duration of the informational component, e.g. $T_r-t_m-t_o$ in the above example. The total duration of all signified levels and additional pulses in the two given selection periods becomes equal to $T_r+t_m-t_o$.

The duration of informational component levels is set in each of the two period T_r in strict accordance with the above rule, while the equalizing voltage levels can be distributed between the two periods arbitrarily following the quasi-reference profile exactly or on average.

What is said above is illustrated in FIG.29, where row control voltages V_{ri} and $V_{r(i+1)}$ and column driving voltage V_{cj} that provides selection to the (ij)-th and (i+1,j) cells are shown over two double-field frames. During each selection period T_r the column receives column-driving voltage pulses containing the informational and equalizing levels, and additional levels containing the t_o-wide reference level V_o and t_m-wide quasi-reference voltages, the amplitude of the latter being equal to that of the basic column-driving voltages. Over each period T_r, the total duration t_{off} of the signified levels with the polarity identical to that of selection pulse V_{ri} and the total duration t_{on} of the signified levels with the polarity opposite to that of selection pulse V_{ri} includes a constant term corresponding to the duration of the additional signified level and may include a variable term corresponding to the sum of durations of quasi-reference equalizing and informational levels. Due to the additional signified levels, signified levels are present in each period T_r. In FIG.29 the signified levels are placed in the beginning and at the end of period T_r. Indices 1 and 2 on terms t_{off} and t_{on} mean whether the signified level belongs to the first or second frame field.

The pixels selected according to the diagram in FIG.29 are supposed to have different levels of brightness: $a_{ij}=-0.5$ and $a_{(i+1)j}=-0.25$. The minus polarity corresponds to level "on". According to the variant of the method, the duration and polarity of the informational level is set $-0.375(T_r-t_m-t_o)$ in the first field and $-0.125(T_r-t_m-t_o)$ in the second. The total duration of each equalizing level for the given pixels makes $0.25(T_r-t_m-t_o)$ over two frame field. The quasi-reference levels of the equalizing component or their fractions can be distributed over intervals T_r in any fashion. In FIG.29 they are all positioned in the second frame fields. As a result, in the first field within the selection period, the total duration of level "off" $t_{off1}=t_m/2$,

and the total duration of level "on" $t_{on1}=t_m/2+0.375(T_r-t_m-t_o)$. In the second field within the selection time, the total duration of level "off" $t_{off2}=t_m/2+0.25(T_r-t_m-t_o)$, and the total duration of level "on" $t_{on2}=t_m/2+0.375(T_r-t_m-t_o)$. The total duration of all signified level in the two given period T_r is $(T_r+t_m-t_o)$.

The examples of the two-field voltage diagrams for pixel couples whose brightness levels correspond to (on, on), (off, off), (gray, gray) given in FIG.17 and FIG.19 have been discussed in the other paragraphs.

The prototype of the tenth variant of the method is given in the US patent 5,489,919 by Asashi Glass Company (the eighth prototype method) in which a multiple-line addressing is offered. FIG.12 shows row-driving voltages for the four-line addressing. The algorithm of finding column voltage levels is given in section "Background of the Invention" for the eighth prototype method. The algorithm consists in successively applying operation "exclusive-or" to logical values corresponding to the row and column voltages, which are constant over period T_r, adding up the results of the operation, and converting the sums into column-driving voltages. The algorithm does not allow pulse-length modulation for the two-line addressing without additional improvements.

The tenth variant of the method differs from the prototype method in the following points:

-two signified level components, informational and quasi-reference equalizing, are applied to the column over period T_r;

-"exclusive-or" logical operation is not performed on logical values corresponding to the row and column voltages, nor is the further summation of the results.

In opposite to the one-line addressing the two-line addressing decreases, according to (17) or (24), the amplitude of the row-driving pulses by a factor of $\sqrt{2}$ and, for many types of display pattern, decreases the cell quasi-ms voltage fluctuations caused by the frame response. As compared to the frame modulation used in the prototype method, the use of the pulse-length modulation also provides a faster frame refresh rate (just in two-field time or in period NT_r) for any gray image gradation.

The tenth variant of the method, especially in combination with other variants, increases the image uniformity and contrast and allows an increased display operation speed and dimensions.

The twelfth embodiment is the eleventh variant of the method of driving a LCD. The LC display is described in the first embodiment. The EOB (electro-optic behavior) of the LCD cell has threshold ms-voltages that set parameter N_{max} equal to or greater than N_{maxo}.

According to (7), $N_{max} \equiv (U_{th1}^2+U_{th2}^2)^2/(U_{th2}^2- U_{th1}^2)^2$ is the display parameter, U_{th1}^2 is the lowest boundary of the working range EOB, U_{th2}^2 is the upper boundary of the said working range. N_{maxo} is the minimal value of N_{max} of the display capable to correct driving by voltage waveforms (by a particular set of driving voltages) in accordance with the variant (or variants) of the method considered. The correct driving must set (or can set) the range of the cell ms voltage corresponding to the working range of the cell EOB. As any driving method allows considerable variations of the cell quasi-ms voltage about the working value, parameters U_{th3} and U_{th4} (see FIG.15) characterize the display parameters in the working mode more exactly and have to be used instead of U_{th1} and U_{th2} for determining N_{maxo}.

Scanning electrodes are selected in one-by-one or group-by-group sequence by applying scanning voltages to the selected scanning electrodes and applying a reference voltage V_o to the non-selected scanning electrodes. During a selection period T_r, basic voltage levels together with additional voltage levels are applied to a signal electrode.

The feature of the variant of the method is the use of row-selection pulses of amplitude $|V_{ro}|\sqrt{1-\eta}$ and column-driving pulses of amplitude $|V_{co}\sqrt{1+\eta}$. Here η is a number that does not exceed number one and is determined by the display parameters by formula $\eta=\sqrt{1-\xi}$. Parameter $\xi = N_{maxo}/N_{max}$ is not greater than one. N_{maxo} is the minimal value of N_{max} that provide correct driving of the display in accordance with a particular timing diagram. $|V_{ro}|$ and $|V_{co}|$ are the modules of the voltages V_r and V_c applied to another (reference) display having the value of N_{max} equal to N_{maxo}, the said other display driven correctly by the variant of the method mentioned. The value η can serve as a parameter for tailoring (adjusting) amplitudes

of voltages V_r and V_c to the values that determine the correct or nearly to correct driving the display having $N_{max} > N_{maxo}$. The value of nearness to correct driving is defined by admissible value of tailoring to best display image. Examples of N_{maxo}, V_{ro}, and V_{co} for a few driving diagrams are given in section "Theoretical backgrounds".

For the display with N_{max} two times greater than N_{maxo} (ξ =0.5) to be correctly driven, the row-selection pulses should have the amplitude of $0.54V_{ro}$ and the column-driving levels should have the amplitude of $1.31V_{c0}$. The result is that the ratio of the amplitude of the quasi-ms voltage fluctuations to the width of the quasi-ms voltage working range (which is defined as $V_{th2}^2-V_{th1}^2$) falls by a factor of 2.3. In the case of the two-line addressing, the use of the variant of the method decreases the amplitude of the quasi-ms voltage fluctuations by a factor of 4.6 as compared to the one-line addressing mode of Alt and Pleshko and allows the dynamic EOB (see FIG.15) to almost fit its static analog.

The prototype of the eleventh variant of the method is the method of one-line-addressing of the display described in the US patent 5,093,736 by Seiko Epson (the seventh prototype method). According to that method, a display with a large number of row electrodes (no less than 300) is driven by row and column voltages with the bias ratio **b** whose value is determined to range from $1/(N^{1/2}-N/200)$ to $1/(N^{1/2}-N/50)$. The aim of this way of driving is to raise the image contrast and display speed of operation.

However, the third paragraph of the theoretical introduction shows that these features of the prototype method can be neither necessary nor sufficient for realizing the declared characteristics of the display.

The variant of the method considered differs from the seventh prototype method in the following points:

- the multiple-line addressing is possible;

- for displays with the number of row electrodes greater than 300, there are not the said range of values within which the "the bias ratio" **b** should vary to generate row and column voltage levels;

- the amplitude of row-selection pulses V_r depends on V_{ro} and N_{maxo}/N_{max} in the above-mentioned manner;

- the amplitude of column-driving pulses V_c depends on V_{co} and N_{maxo}/N_{max} in the above-mentioned manner.

The use of the eleventh variant of the method increases the image contrast without changing the frame rate, improves the image uniformity along row electrode, reduces power consumption, and provides a possibility to raise the display operation speed and dimensions.

The consideration of the variants of the method of driving LC displays that improve their performance finishes at this point.

However, because these variants relate the image quality improving techniques to the display parameters that provide the realization of the declared technical results, the display is further considered as the objects of technical embodiment of the invention.

The thirteenth embodiment of the invention is a LC display. The LC display has a panel including substrates having an array of scanning electrodes on one of substrate and an array of signal electrodes on other substrate. A LC material interposed between the both substrates sets LC cells between the said electrodes at their intersection points. LC cell generates display element of the display and defines change its brightness as a function of the voltage on the cell electrode.

Any of the above variants of the method or their combinations is used to driving. The display is driven using the device described in the seventh embodiment.

The distinguishing point of the display design is that its LC cell generating display element are made with the threshold values of U_{th1}^2 and U_{th2}^2 that set N_{max} no less than N_{maxo}. Here, $N_{max}=(U_{th1}^2+U_{th2}^2)^2/(U_{th2}^2-U_{th1}^2)^2$ is the display parameter comprehensively considered in the text, U_{th1}^2 is the lowest boundary of the working range of the EOB and U_{th2}^2 is the upper boundary of the said working range. N_{maxo} is the minimal value of N_{max} of the display capable to correct driving by a particular set of driving voltages in accordance with the variant (or variants) of the method considered. The correct driving must set the range of the cell ms voltage corresponding to the working range of the cell EOB. In this case, the display can

provide the best image quality. A few values of N_{maxo} for some timing diagrams are given in the theoretical introduction. When the driving of the display is accompanied with considerable variations of the quasi-ms voltage, U_{th3}^2 and U_{th4}^2 of the dynamic EOB (see FIG.15) should be used instead of U_{th1}^2 and U_{th2}^2 for determining N_{max}.

The prototype of this technical solution can be any LC display that is driven using any of the prototype methods considered above.

The display being considered differs from the prototype in that its design should provide N_{max} within a particular range, specifically, it should be no less than N_{maxo}. N_{maxo} is, in turn, dependent on the display timing diagram in a fashion described in the text.

All variants of the driving method (complement each other), the driving device and the display design entering in the invention provide a manifold increase of the image contrast and uniformity, the quality of color rendering, and the display operation speed and dimensions.

As follows from the evaluations, the considered prototype methods in the aggregate are able to reduce the effect of the electric unwanted phenomena in the order of four. This result has not provided sharp enhancing of STN LCD's image quality close to modern TFT LCD's level. The presented multi-variant driving method in the aggregate enables to reduce the effect of such type electric phenomena by a factor of many tens, opening the way to use high-quality STN LCDs on video- and TV-rates. The passive-matrix displays with suppressed cross-talks and other effects be able to have characteristics not only as good as that of active-matrix displays but even surpass them.

Simple design, manufacturability, high image quality and low cost make flat, high-speed color passive-matrix displays a main candidate for cheap and popular television monitors – today's realm of cathode-ray tubes. Active-matrix displays cannot claim this position because of high cost and insufficient speed of rendering small gradations of gray and color.

Brief description of the drawings

FIG.1. A fragment of a LC display coupled to the driving devices.

FIG.2. Volt-brightness behavior of the display element. The first variant.

FIG.3. Volt-brightness behavior of the display element. The second variant.

FIG.4. Timing diagrams of the driving voltages and cell voltages corresponding to the first prototype method without pulse-length modulation.

FIG.5. Timing diagrams of the driving voltages and cell voltages corresponding to the first method with pulse-length modulation.

FIG.6. A timing diagrams of the cell voltage amplitude and the corresponding timing diagrams of the stationary oscillation of the cell quasi-rms voltage.

FIG.7. A cell voltage timing diagram corresponding to the second prototype method.

FIG.8. Timing diagrams of the driving voltages and cell voltages corresponding to the third prototype method.

FIG.9. Timing diagrams of the driving voltages and cell voltages corresponding to the forth prototype method.

FIG.10. Timing diagrams of the driving voltages corresponding to the fifth prototype method without pulse-length modulation.

FIG.11. Timing diagrams of driving voltages for signal electrodes corresponding to the fifth prototype method with pulse-length modulation.

FIG.12. Timing diagrams of row driving voltages for four-line addressing corresponding to the eighth prototype method.

FIG.13. Matrices of row driving voltages for four-line addressing corresponding to the eighth prototype method.

FIG.14. Static square voltage - brightness behavior of a display element (without regard to the "frame response").

FIG.15. Dynamic square voltage - brightness behavior of a display element (with regard to the "frame response").

FIG.16. Timing diagrams for the one-line addressing corresponding to the first embodiment.

FIG.17. Timing diagrams for the two-line addressing corresponding to the first and eleventh embodiments.

FIG.18. Timing diagrams for the one-line addressing corresponding to the first, second, and third embodiments.

FIG.19. Timing diagrams for the two-line addressing corresponding to the first, second, third, and eleventh embodiments.

FIG.20. Timing diagrams for the two-line addressing corresponding to the first, second, third, fourth, and fifth embodiments.

FIG.21. Timing diagrams of pulse shifts for three groups of signal electrodes corresponding to the sixth and third embodiments.

FIG.22. Timing diagrams of pulse shifts for three groups of signal electrodes corresponding to the sixth and fifth embodiments.

FIG.23. A block diagram of the display driving device.

FIG.24. An output circuit diagram of the seventh embodiment.

FIG.25. An output circuit diagram of the seventh embodiment with the additional transistors for adjusting output resistance.

FIG.26. Timing diagrams corresponding to the eighth embodiment.

FIG.27. Timing diagrams corresponding to the ninth embodiment.

FIG.28. The shapes of voltage pulses corresponding to the tenth embodiment.

FIG.29.Timing diagrams corresponding to the eleventh embodiment with pulse-length modulation.

The best way to implement the invention

The technical solutions considered in the patent application are feasible. Since the variants of the method offered correlate well with each other, the best way to implement the invention is to use all or nearly all of these technical solutions.

The examples of the joint application of the variants of the method and the results thus achieved are given in the appropriate paragraphs and illustrated in the corresponding figures.

Feasibility

The invention can be used for producing video monitors in computer and television industry.

The block diagram of the display driving device that can realizes the driving voltages and timing diagrams in accordance with the variants of the method offered is shown in FIG.23. The timing diagrams for a particular row are formed in logical blocks LB_i with the help of conventional methods. The logical block can include

trigger elements, shift registers, and other circuits and have various designs. For any driving method (including the seventh method, which have different timing diagrams for different channels), the logic blocks form the row timing diagrams that are independent of particular image pattern.

When the seventh and eighth variants of the driving method are used, the voltage levels dependent on the channel number are formed in the voltage level generator at the tuning stage. This case, the number of voltage levels is growing.

The timing diagrams for a particular column electrode are generated in the logic blocks LB_j. What has been said about LB_i remains true for LB_j. In contrast to LB_i, LB_j have additional circuits realizing the pulse-length modulation of the column-driving levels. For pulse-length modulation to be realized for the two-line addressing in accordance with the tenth control method, logic blocks LBj can incorporate additional register and summing circuits that perform summation or subtraction of data signals relating to two concurrently selected pixels of the neighboring row electrodes, as well as register and summing circuits designed for determining the compensating quasi-reference voltages. It is also possible to use other designs where summation/subtraction of data signals and determining the durations of compensating pulses are realized in the data processing unit (this unit is not shown in FIG.23) whose output data signals go to block 3 by data buses.

According to the sixth driving method, for the voltage pulses to be applied to different signal electrodes at different moments, logic units LB_j or a clock pulse generator (this unit is not shown in FIG.23) can incorporate pulse delay elements or circuits.

For the driving pulses to have the stepped leading edges (which is needed for implementing the ninth driving method), the voltage generator 1 yields additional voltage levels which are switched by logic units in accordance with specific timing diagrams. The voltage levels can be switched, for instance, in voltage converter blocks VCB_i (FIG.23) before being applied to the transistor leads 13 and 14 (FIG.24 or FIG.25).

For displays with N_{max} greater than N_{maxo}, according to the eleventh method the row and column voltage levels are formed and set in the voltage generator 1.

The feasibility of the device according to the seventh embodiment arises from its description.

The device that generates the driving voltages according the timing diagrams described in the variants of the invention can be realized using driver circuits or on the display panel.

The feasibility of the approach presented in section "Disclosing of the Invention" results from its subsection "Theoretical background", appropriate formulae, and numerical estimations.

WHAT IS CLAIMED IS:

1. A method of driving a display having a panel including substrates having an array of scanning electrodes on one of substrate, an array of signal electrodes on other substrate, and liquid crystal cells between the said electrodes at their intersection points, the said cells generating display elements of the display, comprising the steps of:

selecting scanning electrodes in one-by-one or group-by-group sequence, applying scanning voltages to the selected scanning electrodes, and applying a reference voltage (V_o-level) to the non-selected scanning electrodes;

applying, during a selection period, a basic voltage level or levels consisting of a level or levels unequal to V_o-level or/and of V_o-level to a signal electrode for obtaining current values of brightness of a selected display element or of a group of selected display elements; the distinguishing step of:

applying, during the selection period, two additional voltage levels having different polarities, the same constant modules of deviation from V_o-level, and constant and equal duration to the signal electrode.

2. A method of driving a display having a panel including substrates having an array of scanning electrodes on one of substrate, an array of signal electrodes on other substrate, and liquid crystal cells between the said electrodes at their intersection points, the said cells generating display elements of the display, comprising the steps of:

selecting scanning electrodes in one-by-one or group-by-group sequence, applying scanning voltages to the selected scanning electrodes, and applying a reference voltage (V_o-level) to the non-selected scanning electrodes;

applying, during a selection period (T_r), a basic voltage level or levels consisting of a level or levels unequal to V_o-level or/and of V_o-level to a signal electrode for obtaining current values of brightness of a selected display element or of a group of selected display elements; the distinguishing steps of:

applying, during the period T_r, two additional voltage levels having different polarities, the same constant modules (V_m) of deviation from V_o-level, and constant and equal duration ($t_m/2$) to the signal electrode;

applying, during the period T_r after applying a voltage of one polarity about V_o-level and before applying a voltage of other polarity about V_o-level, the third additional V_o-voltage level having a constant duration (t_o) to the signal electrode.

3. The method of claim 2, wherein durations of the basic voltage levels applying to the signal electrode are varied for obtaining a particular current value of brightness of the selected display elements and are adjusted in such a way

that under one-line selection, during period T_r, the sum duration of all basic voltage levels is equal to constant value ($T_r - t_m - t_o$) or,

that under multiple-line selection, during all periods of selection the same display elements in frame time, the averaged over period T_r sum of products of duration of every basic voltage level unequal to V_o to square of inverted ratio of modulus of deviation of the said level from V_o-level to modulus of deviation (from V_o-level) of the basic level for the said display one-line selected by the said method (with the same values $t_m/2$ and V_m of the said pair of additional levels and with the same duration t_o of the said third additional V_o-level) is equal to constant value ($T_r - t_m - t_o$).

4. A method of driving a display having a panel including substrates having an array of scanning electrodes on one of substrate, an array of signal electrodes on other substrate, and liquid crystal cells between the said electrodes at their intersection points, the said cells generating display elements of the display, comprising the steps of:

selecting scanning electrodes in one-by-one or group-by-group sequence, applying scanning voltages to the selected scanning electrodes, and applying a reference voltage (V_o-level) to the non-selected scanning electrodes;

applying, during a selection period (T_r), a basic voltage level or levels consisting of a level or levels unequal to V_o-level or/and of V_o-level to a signal electrode for obtaining current values of brightness of a selected display element or of a group of selected display elements; the distinguishing steps of:

applying, during the period T_r, two additional voltage levels having different polarities, the same constant modules of deviation from V_o-level, and constant and equal duration to the signal electrode, the said additional voltage levels being

allocated to the boundary portions of the period T_r so that one level is allocated to the beginning portion and the other level is allocated to the end portion of the period T_r;

applying, during the period T_r, voltage levels to the signal electrode in direct or in reverse order; and

alternating, in succeeding periods T_r, the said orders of applying of voltage levels to the signal electrode on the basis of changing of the polarity of the voltage deviation from V_o- level in the beginning (and, accordingly, in the end) of the period T_r so that the positive polarity being set in the beginning of one period T_r and the negative polarity being set in the beginning of the next period T_r.

5. A method of driving a display having a panel including substrates having an array of scanning electrodes on one of substrate, an array of signal electrodes on other substrate, and liquid crystal cells between the said electrodes at their intersection points, the said cells generating display elements of the display, comprising the steps of:

selecting scanning electrodes in one-by-one or group-by-group sequence, applying scanning voltages to the selected scanning electrodes, and applying a reference voltage (V_o-level) to the non-selected scanning electrodes;

applying, during a selection period (T_r), a basic voltage level or levels consisting of a level or levels unequal to V_o-level or/and of V_o-level to a signal electrode for obtaining current values of brightness of a selected display element or of a group of selected display elements; the distinguishing steps of:

applying, during the period T_r, two additional voltage levels having different polarities, the same constant modules of deviation from V_o-level, and constant and equal duration to the signal electrode, the said additional voltage levels being allocated to the boundary portions of the period T_r so that one level is allocated to the beginning portion and the other level is allocated to the end portion of the period T_r;

applying, during the period T_r, voltage levels to the signal electrode in direct or in reverse order; and

applying, during the period T_r, voltage levels to adjacent signal electrodes or to signal electrodes located one or two electrodes further or to signal electrodes having another type of activation sequence so that the levels allocated to the beginning

portion (and, accordingly, to the end portion) of the period T_r have deviations of opposite polarities from V_o-level.

6. A method of driving a display having a panel including substrates having an array of scanning electrodes on one of substrate, an array of signal electrodes on other substrate, and liquid crystal cells between the said electrodes at their intersection points, the said cells generating display elements of the display, comprising the steps of:

selecting scanning electrodes in one-by-one or group-by-group sequence, applying scanning voltages (V_r) to the selected scanning electrodes, and applying a reference voltage (V_o-level) to the non-selected scanning electrodes;

applying, during a selection period (T_r), a basic voltage level or levels consisting of a level or levels unequal to V_o-level or/and of V_o-level to a signal electrode for obtaining current values of brightness of a selected display element or of a group of selected display elements; the distinguishing steps of:

applying, during the period T_r, two additional voltage levels having different polarities, the same constant modules of deviation from V_o-level, and constant and equal duration to the signal electrode, the said additional voltage levels being allocated to the boundary portions of the period T_r so that one level is allocated to the beginning portion and the other level is allocated to the end portion of the period T_r;

applying, during the period T_r, voltage levels to the signal electrode in direct or in reverse order; and

alternating, during periods T_r of selecting the same scanning electrode or the same group of scanning electrodes where the scanning voltages or the scanning voltage groups have identical or opposite polarities about V_o-level, the said order of the applying the signal voltage levels to the signal electrode (during period T_r) in succeeding frame time periods or in a frame time or in two frame time or in accord with other order of comparison in time by setting alternately the same and opposite directions of the deviation (from V_o-level) of the signal voltage level allocated to the beginning (and, accordingly, to the end) portion of the period T_r and of the deviation (from V_o-level) of the voltage V_r applied to the said same selected scanning electrode or to the same selected scanning electrode of the said same selected group.

7. A method of driving a display having a panel including substrates having an array of scanning electrodes on one of substrate, an array of signal electrodes on other substrate, and liquid crystal cells between the said electrodes at their intersection points, the said cells generating display elements of the display, comprising the steps of:

selecting scanning electrodes in one-by-one or group-by-group sequence, applying scanning voltages to the selected scanning electrodes, and applying a reference voltage (V_o-level) to the non-selected scanning electrodes;

applying, during a selection period (T_r), pulses of voltage to signal electrode, the said pulses setting a basic voltage level or levels consisting of a level or levels unequal to V_o-level or/and of V_o-level for obtaining current values of brightness of a selected display element or of a group of selected display elements; the distinguishing steps of:

applying, during the period T_r, two additional voltage levels having different polarities, the same constant modules of deviation from V_o-level, and constant and equal duration ($t_m/2$) to the signal electrode, the said additional voltage levels being allocated to the boundary portions of the period T_r so that one level is allocated to the beginning portion and the other level is allocated to the end portion of the period T_r;

applying, during the period T_r, voltage levels to the signal electrode in direct or in reverse order so that the order of their applying to the signal electrode is alternated in succeeding periods T_r; and

splitting the voltage pulses applied to signal electrodes into a number of groups being related to different electrodes and shifting the pulses in time concerning their nominal positions in the period T_r so that the values of shifting time are the same for the pulses of a single group, but are different for the pulses of different groups, and constant for certain period, after termination the said time period, other values of shifting time are set in certain or in all groups of voltage pulses or other aggregate of groups of voltage pulses is formed with different values of shifting time in various groups, and the other values of shifting time are set constant for the next time period, after termination of which the said process of either changing or setting constant

values of shifting time are continued providing zero average deviation of duration of each said additional level from its nominal duration.

8. The method of claim 7, wherein modulus of shifting times of voltage pulses applied to a group of the signal electrodes are set in the range of values from zero to $t_m/2$.

9. The method of claim 7, wherein, after termination of the time period during which the shifting time values of groups of voltage pulses applied to the signal electrodes are kept constant, the latest shifting time value are set in the group of pulses, each having the earliest shifting time value, the previous shifting time value is set in the group of pulses, each having the next after the earliest shifting time value, and such changing of shifting time values is applied in other groups up to group of pulses, each having the earliest shifting time value, which are changed to the latest shifting time value.

10. The method of claim 7, wherein a group of voltage pulses having the same shifting time is formed for a group of signal electrodes in such a way that each electrode is distant from other electrodes in the group.

11. A method of driving a display having a panel including substrates having an array of scanning electrodes on one of substrate, an array of signal electrodes on other substrate, and liquid crystal cells between the said electrodes at their intersection points, the said cells generating display elements of the display, comprising the steps of:

selecting scanning electrodes in one-by-one or group-by-group sequence, applying pulses of scanning voltages to the selected scanning electrodes, and applying a reference voltage (V_o-level) to the non-selected scanning electrodes;

applying, during a selection period, pulses of voltage to signal electrode, the said pulses setting a basic voltage level or levels consisting of a level or levels unequal to V_o-level or/and of V_o-level, the said levels setting nominal values of mean square voltage on the selected cell or cells for obtaining current values of brightness of a selected display element or of a group of selected display elements; the distinguishing steps of:

applying, during the selection period, two additional voltage levels having different polarities, the same constant modules of deviation from V_o-level, and constant and equal duration to the signal electrode, the said additional levels setting practically constant (in time) deviations from the nominal values of mean square voltage on cells connected with the signal electrode, the said deviations being caused by distortions of a shape of the voltage pulses in process of their propagation along the signal electrode;

providing, during a frame time period, a single or several additional time intervals (t_c);

applying, during some mentioned single or several intervals t_c, compensative voltages $V_{com}(i)$ to each i-th scanning electrode, beginning with a certain electrode, or/and during other mentioned single or several intervals t_c, applying compensative voltages V_{com} (j) to each j-th signal electrode, beginning with other certain electrode, the said voltages V_{com} (i) or/and, respectively, V_{com} (j) having values or/and durations specific to each electrode and giving the total or a partial compensation of the deviations of the mean square voltages on the sells of the i-th scanning electrode from their nominal values or/and, respectively, of the deviations of the mean square voltages on the sells of the j-th signal electrode from their nominal values, the said deviations initiated by the said distortions of shape of the signal voltage pulses in process of their propagation along the signal electrode, or/and, respectively, initiated by distortions of shape of the scanning voltage pulses in process of their propagation along the scanning electrode; and

applying, during the mentioned intervals t_c, the reference voltage or a quasi-reference voltage or a quasi-reference voltage on average or their combination to the scanning or/and to the signal electrodes free from the said compensative voltages.

12. A method of driving a display having a panel including substrates having an array of scanning electrodes on one of substrate, an array of signal electrodes on other substrate, and liquid crystal cells between the said electrodes at their intersection points, the said cells generating display elements of the display, comprising the steps of:

selecting scanning electrodes in one-by-one or group-by-group sequence, applying scanning voltages to the selected scanning electrodes, and applying a reference voltage (V_o-level) to the non-selected scanning electrodes;

applying, during a selection period, a basic voltage level or levels consisting of a level or levels unequal to V_o-level or/and of V_o-level to a signal electrode , the said levels setting nominal values of mean square voltage on the selected cell or cells for obtaining current values of brightness of a selected display element or of a group of selected display elements; the distinguishing steps of:

applying, during the selection period, two additional voltage levels having different polarities, the same constant modules of deviation from V_o-level, and constant and equal duration to the signal electrode, the said additional levels setting practically constant (in time) deviations from the nominal values of mean square voltage on cells connected with the signal electrode, the said deviations being caused by distortions of a shape of the voltage pulses in process of their propagation along the signal electrode;

applying, during the selection periods, additional compensative voltages to selected scanning electrodes, beginning with a certain electrode, and superimposing the said compensative voltage on the scanning voltage, the said compensative voltage having value or/and duration specific to the selected scanning electrode and total or a partial compensating the deviations of the mean square voltages on the cells of the selected scanning electrode from their nominal values, the said deviations being caused by the said distortions of shape of the signal voltage pulses in process of their propagation along the signal electrode.

13. A method of driving a display having a panel including substrates having an array of scanning electrodes on one of substrate, an array of signal electrodes on other substrate, and liquid crystal cells between the said electrodes at their intersection points, the said cells generating display elements of the display, comprising the steps of:

selecting scanning electrodes in one-by-one or group-by-group sequence, applying pulses of scanning voltages to the selected scanning electrodes, and applying a reference voltage (V_o-level) to the non-selected scanning electrodes;

applying pulses of voltage to signal electrode, the said pulses setting basic voltage level or levels setting nominal values of mean square voltage on selected sells for obtaining nominal values of brightness of selected display elements; the distinguishing step of:

forming voltage pulses in the shape providing total or partial self-compensation of spurious changes of the mean square voltages on the selected sells, the said changes initiated by distortions of fronts and tails of the pulses in process of their propagation along display electrode.

14. The method of claim 13, wherein the front of pulse is formed in stepwise shape or in the shape similar to stepwise one.

15. A method of driving a display having a panel including substrates having an array of scanning electrodes on one of substrate, an array of signal electrodes on other substrate, and liquid crystal cells between the said electrodes at their intersection points, the said cells generating display elements of the display, comprising the steps of:

selecting scanning electrodes two times or more times a frame in sequence two by two, applying scanning voltages (V_{r1} and V_{r2}) to selected scanning electrodes, and applying a reference voltage (V_o-level) to the non-selected scanning electrodes, wherein polarities of deviation voltages V_{r1} and V_{r2} from V_o-level are set either same or opposite (or in reverse order, or in mixed order);

applying, during a selecting period (T_r), a basic voltage level or levels having the same modulus Vc of deviation from V_o-level or/and of V_o-level to a signal electrode for obtaining current values of brightness of selected display elements; and the distinguishing step of:

forming the said unequal to V_o-level basic voltage levels being composed of an information component and of quasi-reference equalizing components such

that the duration and the polarity of deviation from V_o-level of the information component, during the period T_r of the applying the scanning voltages V_{r1} and V_{r2} with the same polarities of deviation from V_o-level, being set in ratio to the value of half sum of brightness of the selected display elements (or with correction of the ratio

taking into account an non-linearity of an electro-optic behavior of the display element),

that the duration and the polarity of deviation from V_o-level of the information component, during the period T_r of the applying the scanning voltages V_{r1} and V_{r2} with opposite polarities of deviation from V_o-level, being set in ratio to the value of half difference between brightness of the selected display elements (or with the said correction of the ratio taking into account the said non-linearity), and

that the common duration of the quasi-reference equalizing components being set, during any or both periods T_r in the frame of selecting the same display elements, to bring the common duration of all levels unequal to V_o (for the said same selected display elements) to constant value.

16. The method of claim 15 including claim 1, wherein the said constant value of common duration of all signal voltages levels unequal to Vo and applied to the signal electrode for the same elements selected in both periods T_r of the frame, the levels including information component, equalizing component, and two additional levels with different polarities, constant modules of deviation from V_o-level equal to V_c, and constant and equal duration ($t_m/2$), the said additional levels set during every period T_r, is equal to (T_r+t_m).

17. A device for driving a display having a panel including substrates having an array of scanning electrodes on one of substrate, an array of signal electrodes on other substrate, and liquid crystal cells between the said electrodes at their intersection points, the said cells generating display elements of the display, the display driven by the method variants of claims from 1 to 16 realized separately or in their combinations, comprising:

a voltage level generator (or power supply block) and a bunch of voltage pulsers for the display electrodes, each voltage pulser containing a block setting timing voltage levels to an output electrode, the output electrode, and an output transistor block connected with the output electrode, with the voltage level generator and with the block setting timing voltage levels connected with the voltage level generator, characterized in that

the block setting timing voltage level to the output signal electrode contains technical means to timing additional voltage levels of constant duration, applying to the signal electrode; and

the output transistor block is fixed in such a way that the output resistances for different voltage levels of the said block has the same values, or the deviation of values does not exceed 10%.

18. A method of driving a display having a panel including substrates having an array of scanning electrodes on one of substrate, an array of signal electrodes on other substrate, and liquid crystal cells between the said electrodes at their intersection points, the said cells generating display elements of the display, having value of display parameter N_{max} greater or equal to number N_{maxo}, where N_{maxo} is the minimum value of N_{max} of the display capable to correct driving by voltage waveforms in accordance with the method variants of claims from 1 to 16, realized separately or in their combination, comprising the steps of:

selecting scanning electrodes in sequence one by one or group by group, applying scanning voltages (V_r) to the selected scanning electrodes, and applying a reference voltage (V_o-level) to the non-selected scanning electrodes;

applying, during a selecting period, a basic voltage level or levels (Vc) consisting of a level or levels unequal to V_o-level or/and of V_o-level to a signal electrode for obtaining current values of brightness of a selected display element or of a group of selected display elements; and the distinguishing steps of:

applying the voltages V_r about $|V_{ro}|\sqrt{1-\eta}$ to the scanning electrodes,

applying the voltages V_c about $|V_{co}|\sqrt{1+\eta}$ to the signal electrodes,

wherein $|V_{ro}|$ and $|V_{co}|$ are the modules of the voltages V_r and V_c applied to another (reference) display having the value of N_{max} equal to N_{maxo}, the said other display driven correctly by the method of the mentioned claims, and η is a number parameter for tailoring of the voltages V_r and V_c to the correct driving or close to the correct driving of the said display having N_{max} greater or equal to N_{maxo}.

19. A display having a panel including substrates having an array of scanning electrodes on one of substrate, an array of signal electrodes on other substrate, and liquid crystal cells between the said electrodes at their intersection points, the said cells generating display elements of the display, characterized in that

the display elements are made having the value of display parameter N_{max} greater or equal number N_{maxo}, where N_{maxo} is greater number N and N_{maxo} is the minimum value of N_{max} of a display capable to correct driving by voltage waveforms in accordance with the method variants of claims from 1 to 16, realized separately or in their combination.

ABSTRACT

During the selection period T_r, display column electrodes receive two additional identical voltage levels whose polarities are symmetric about the reference voltage V_o and the third additional V_o-level of constant duration applying between the voltage levels of different polarities. The additional opposite-polarity levels allocated to the boundary portions of the period T_r. All levels are applied to the signal electrode in direct or in reverse order. The allocation of the levels alternates in succeeding periods T_r, on adjacent column electrodes, in succeeding frame periods. The voltage pulses to signal electrodes are split into a groups being related to different electrodes and shifted in time. The shifting times are changed in the course of time (Fig.21). The driving device incorporates output block which output resistances for different voltage levels have the same values. The display electrodes receive a compensation voltages that are independent of image patterns. The pulse shapes provide self-compensation of spurious changes of the mean square voltages on LC sells. For the two-line addressing mode, column-driving voltages have the informational and quasi-reference equalizing components. Row and column driving voltages are set equal to $|V_{ro}|\sqrt{1-\eta}$ and $|V_{co}|\sqrt{1+\eta}$, where η is the voltage adjustment parameter. N_{max} of the display is no less than N_{maxo} determined for a particular voltage-timing diagram. All embodiments of the invention are complement each other. The aim is to improve drastic the image uniformity and contrast, and to increase of the display size and operation speed.

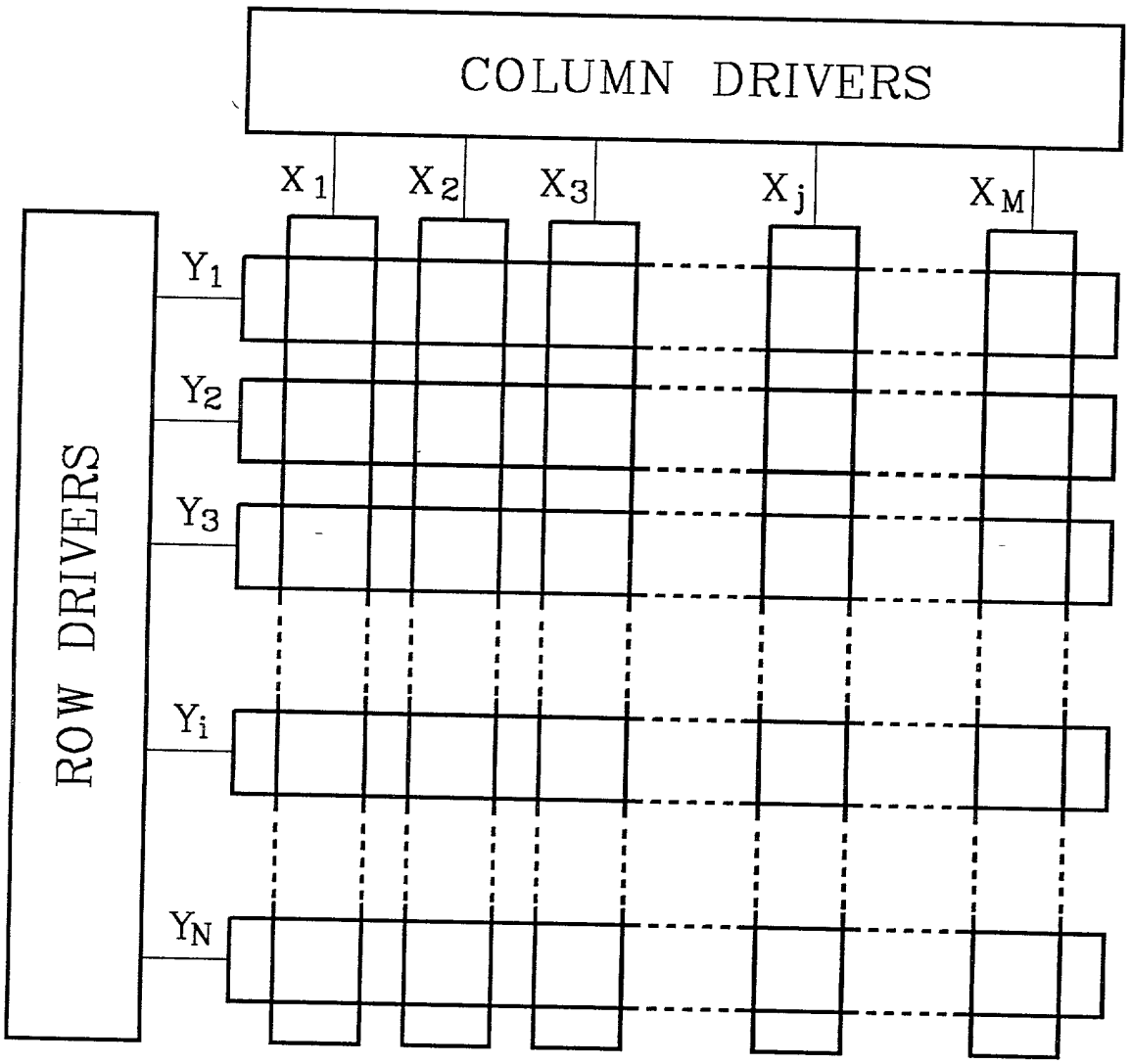

FIG. 1

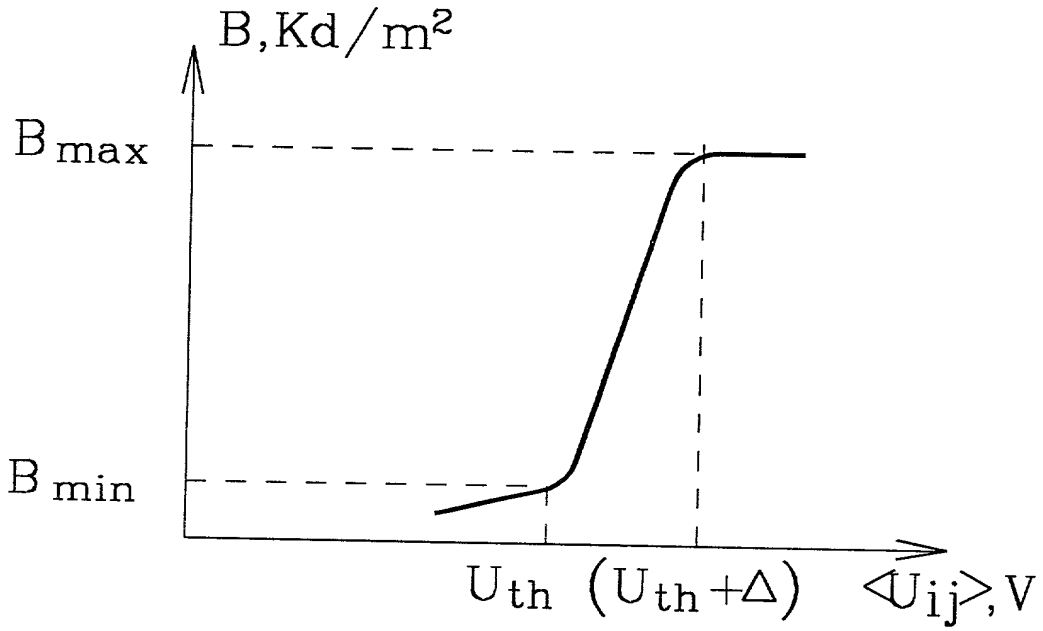

FIG. 2

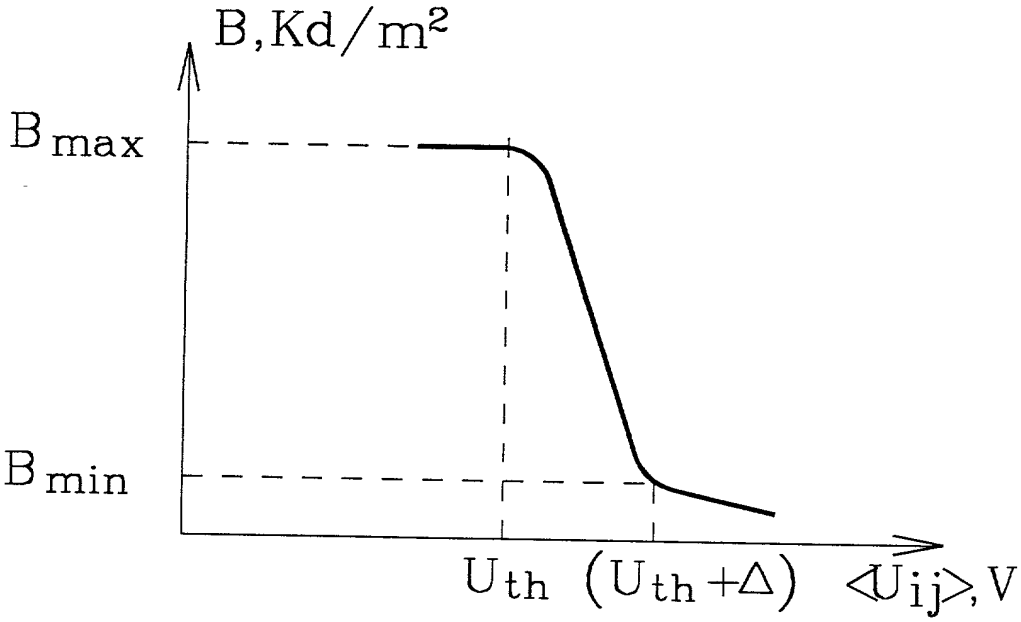

FIG. 3

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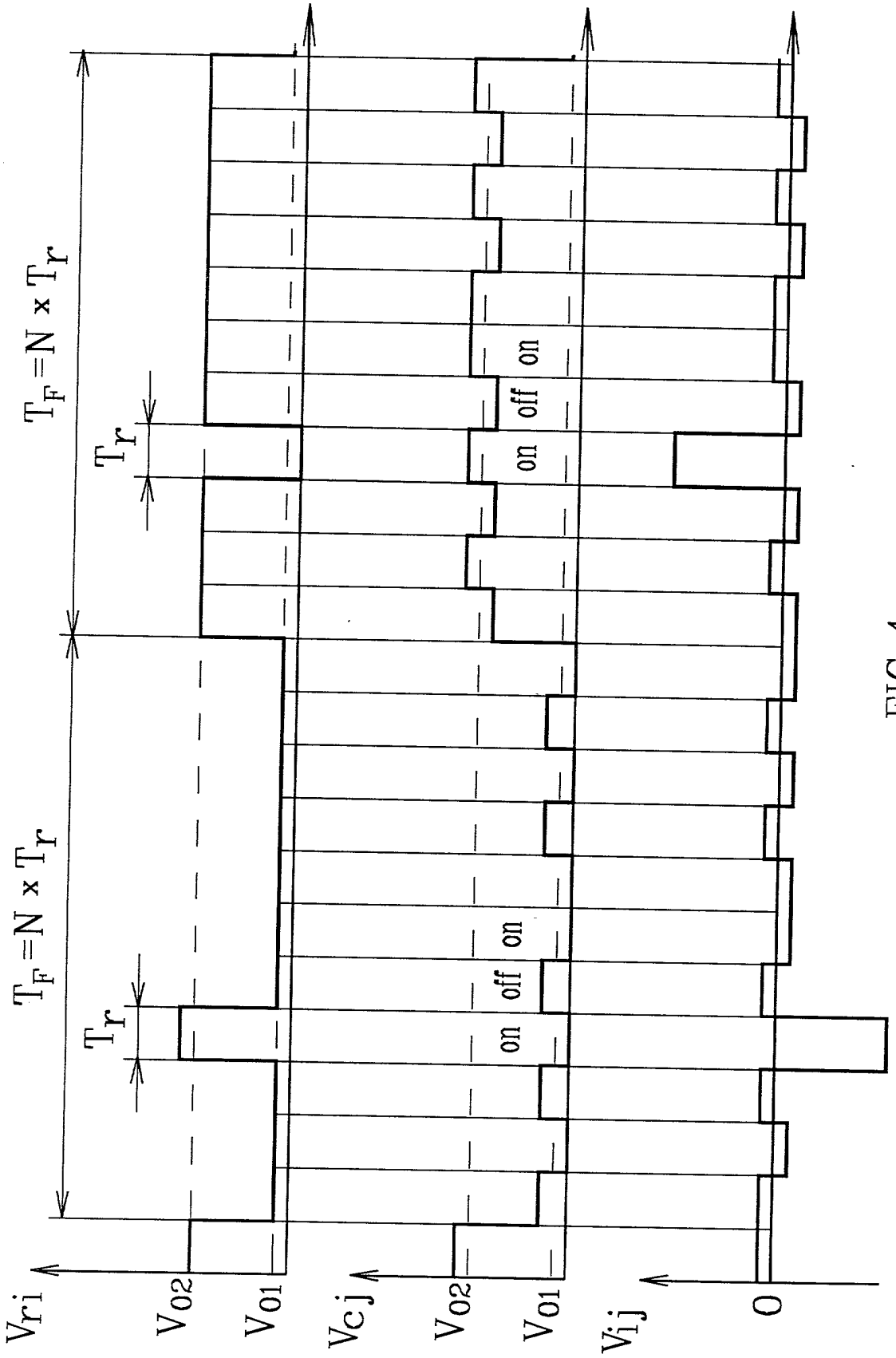

FIG. 4

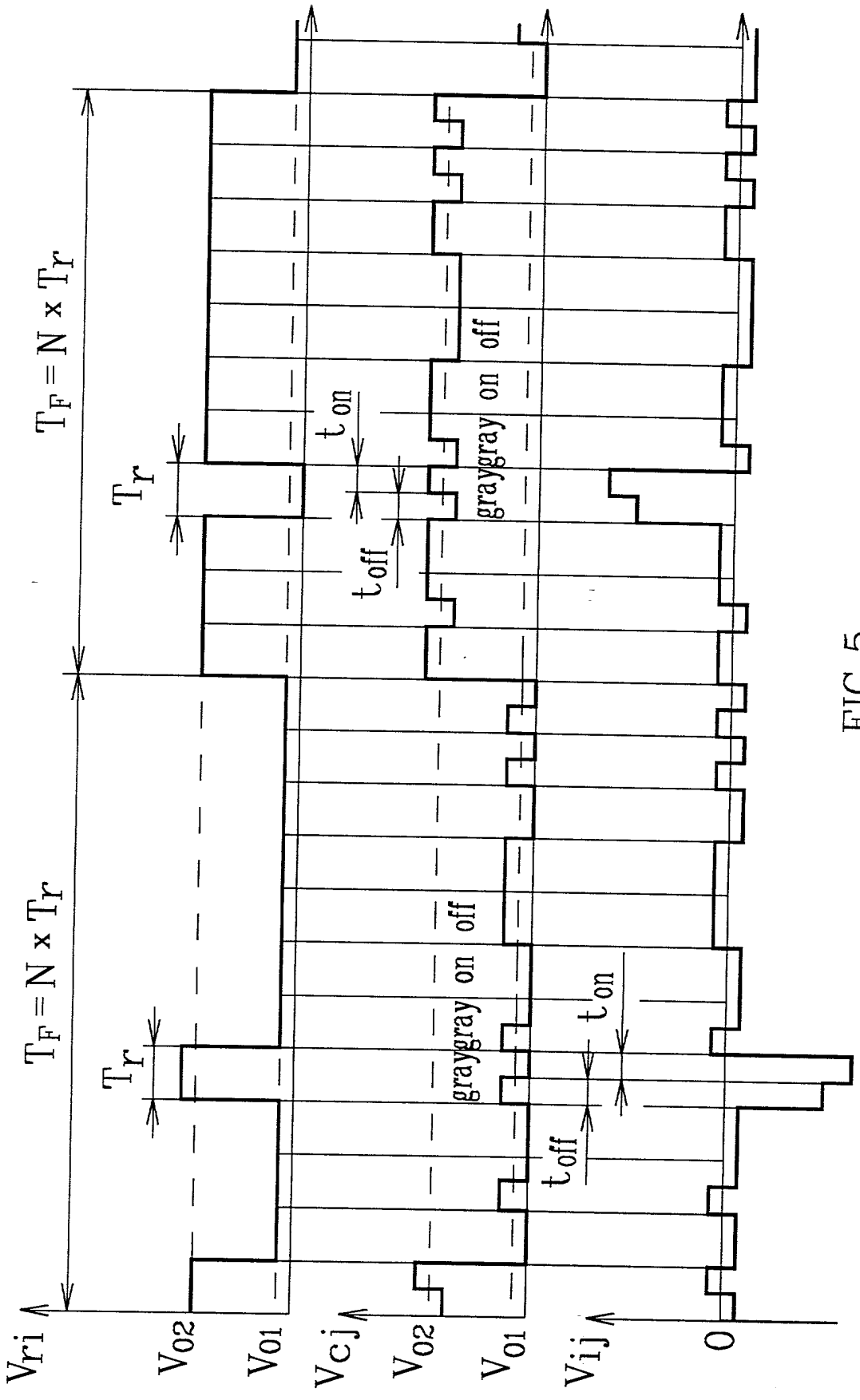

FIG.5

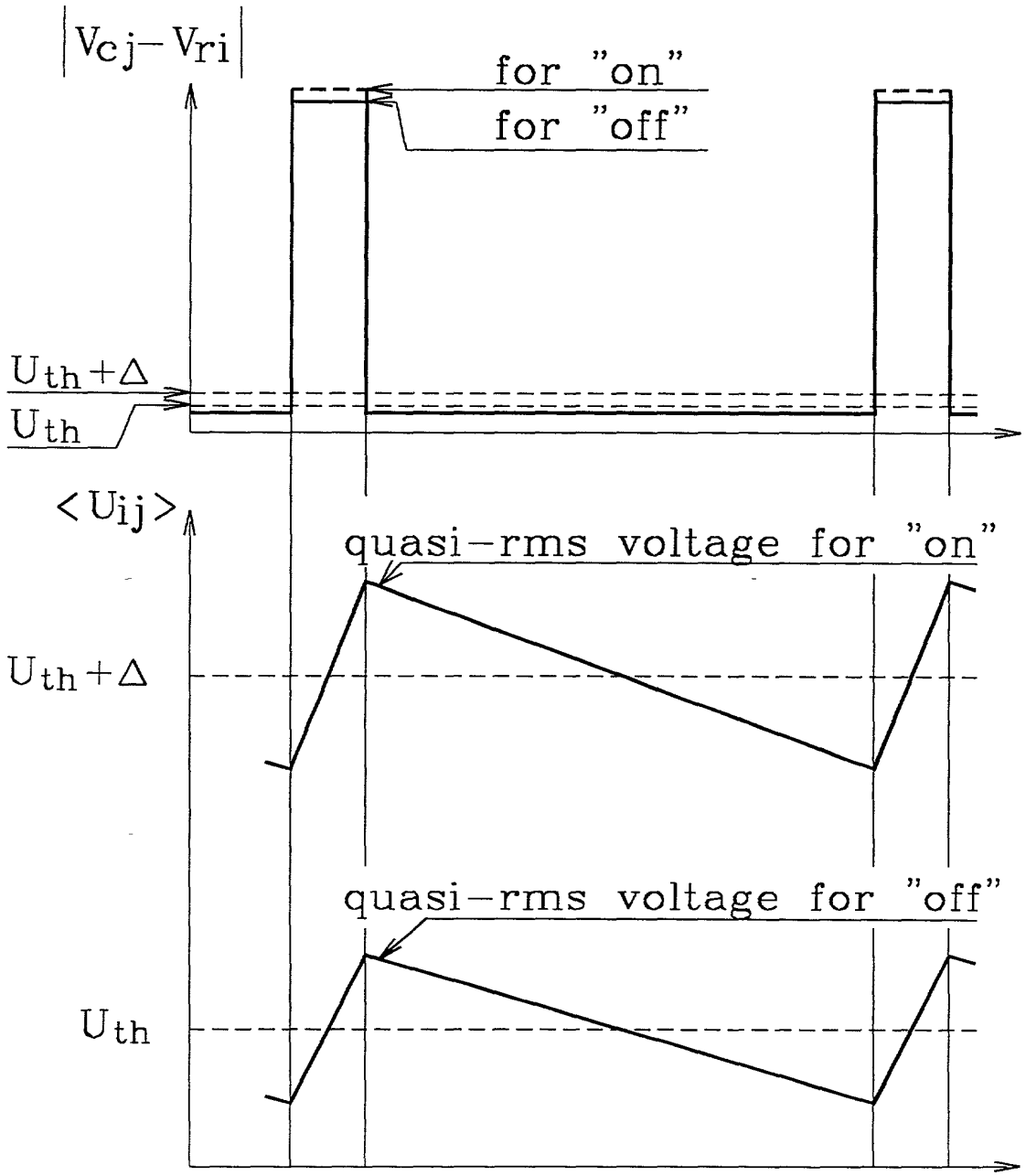

FIG.6

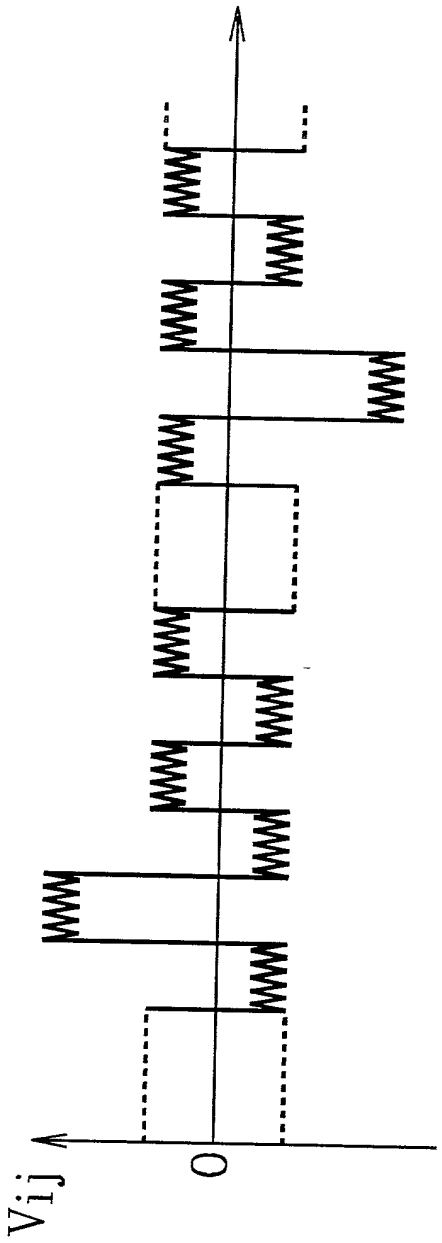

FIG. 7

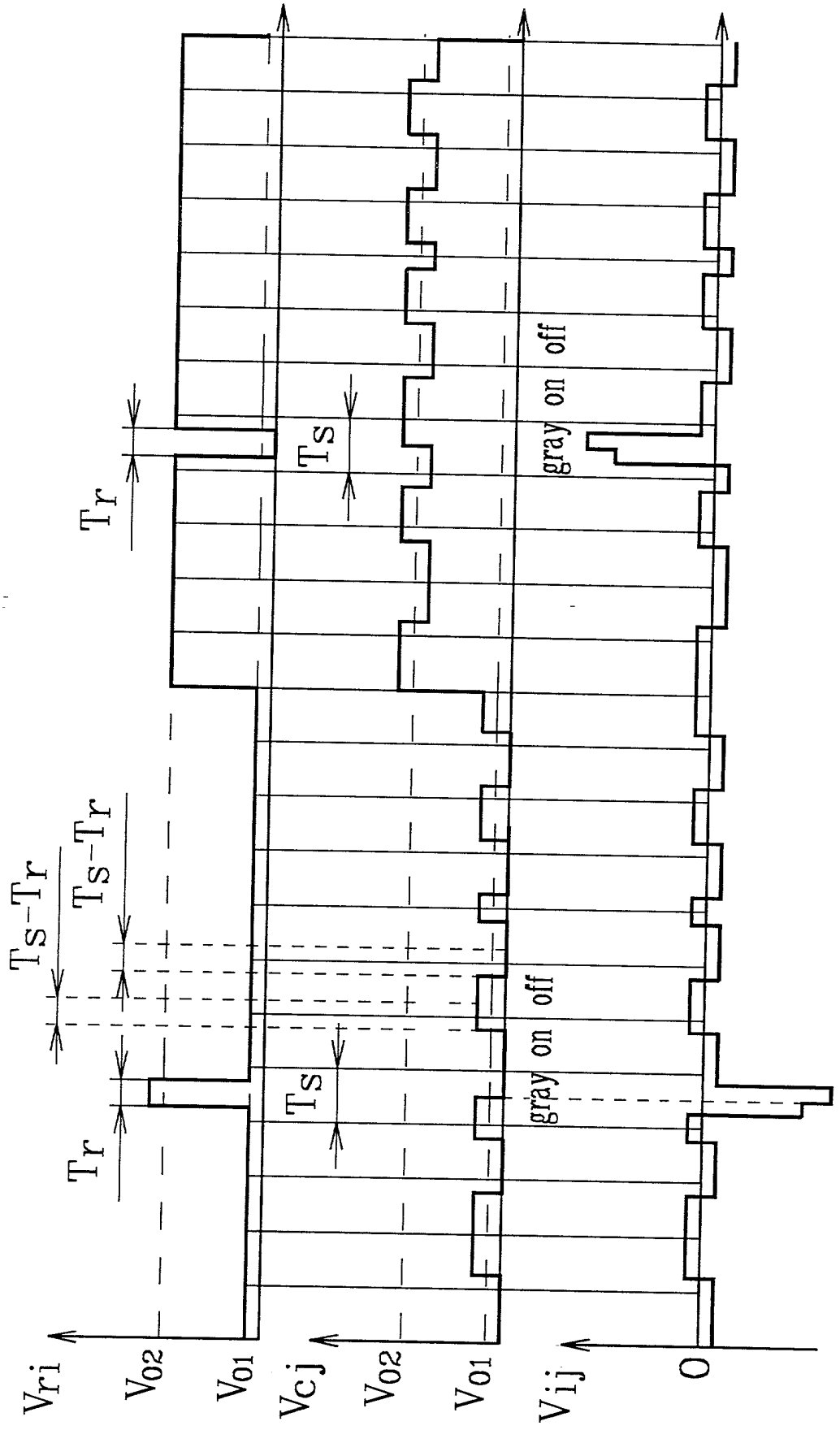

FIG. 8

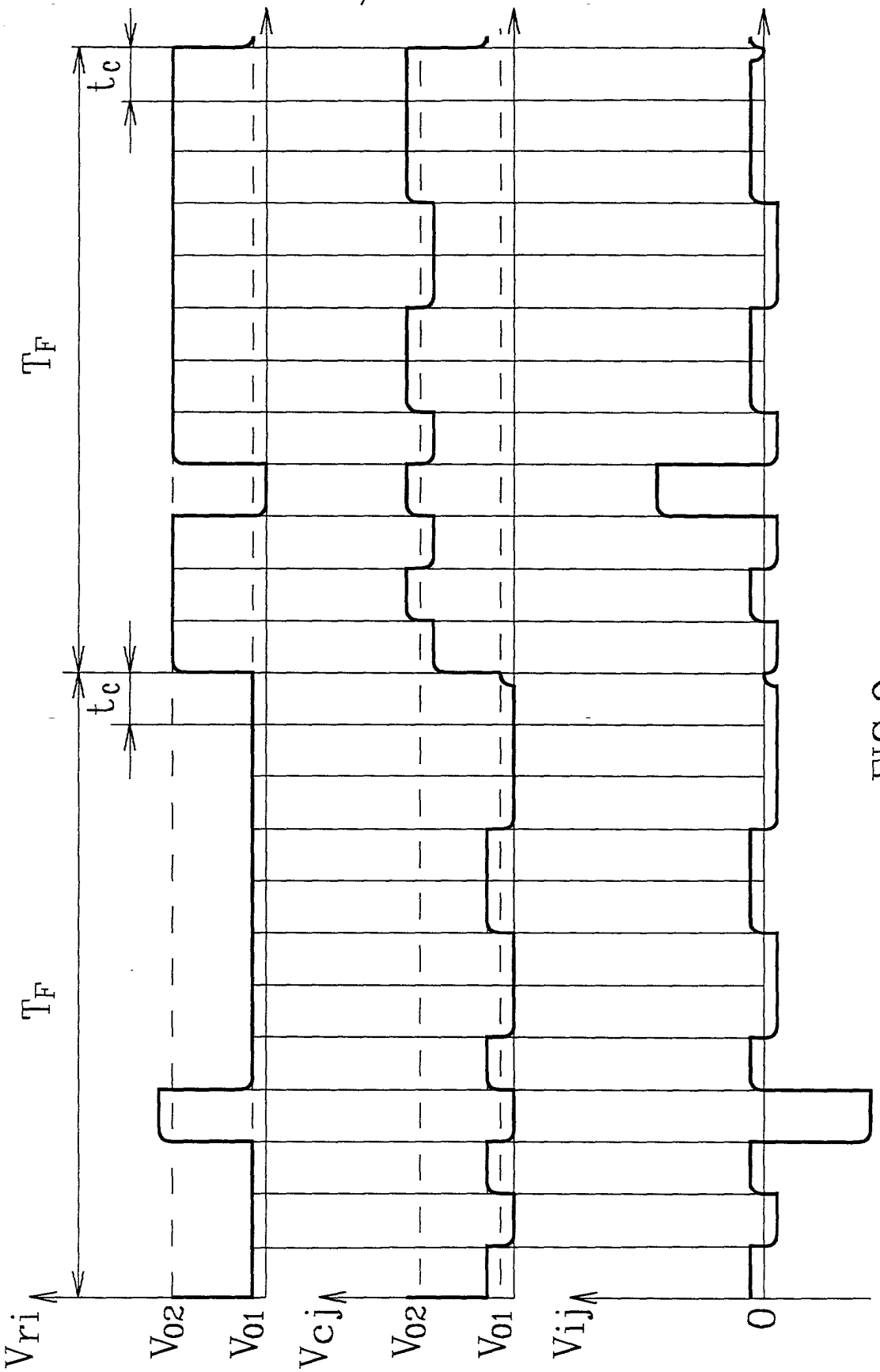

FIG. 9

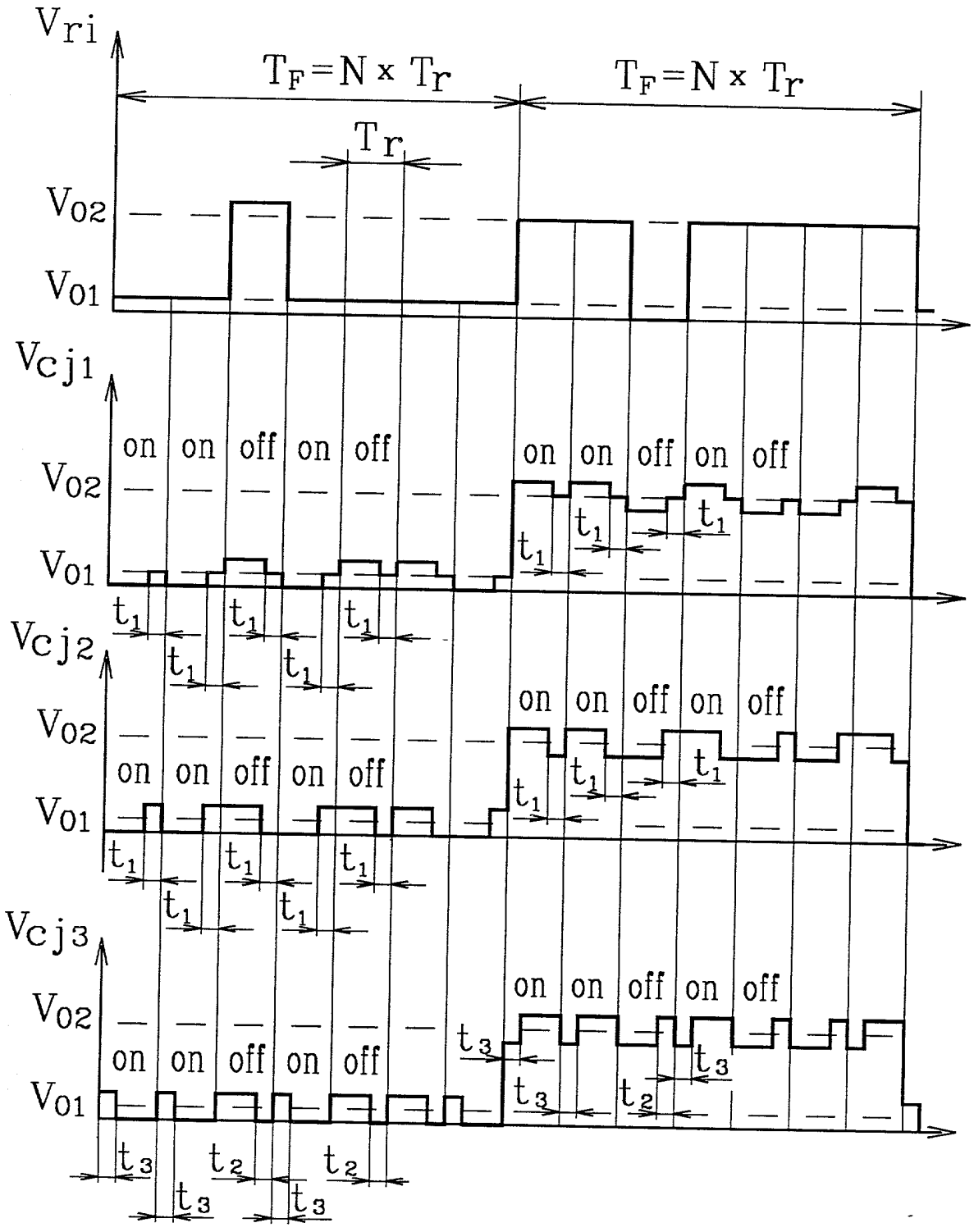

FIG.10

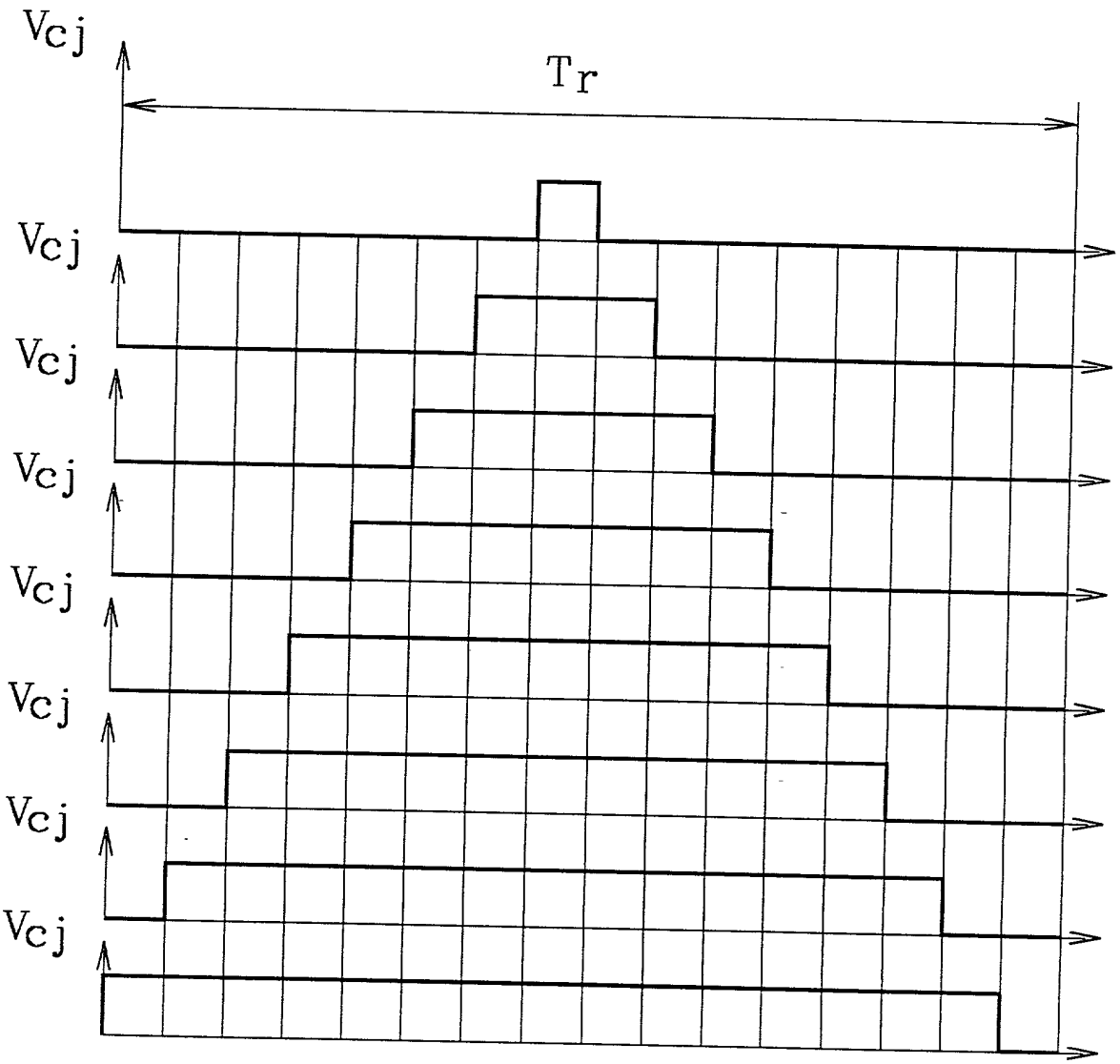

FIG. 11

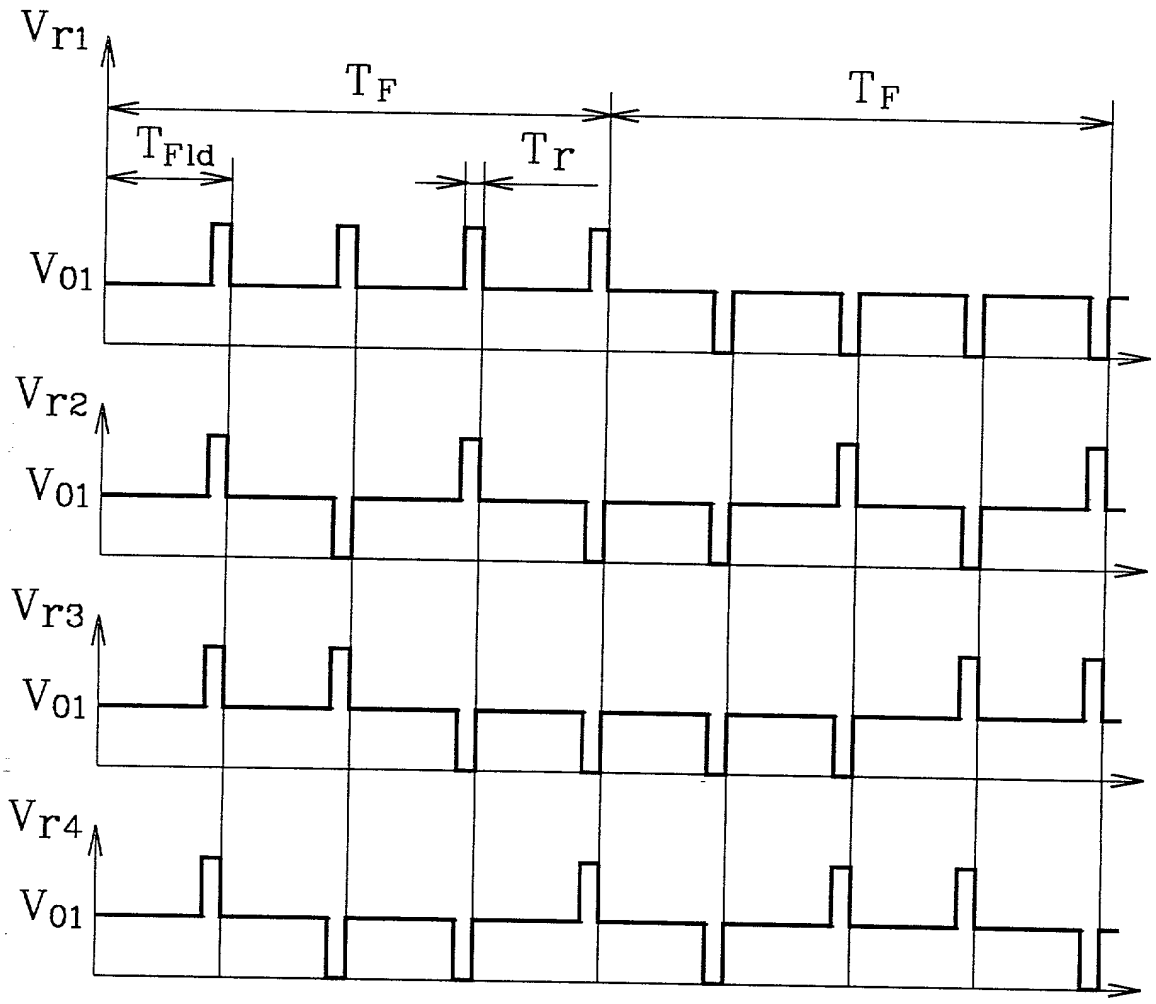

FIG.12

$$\begin{pmatrix} 1 & 1 & 1 & 1 & -1 & -1 & -1 & -1 \\ 1 & -1 & 1 & -1 & -1 & 1 & -1 & 1 \\ 1 & 1 & -1 & -1 & -1 & -1 & 1 & 1 \\ 1 & -1 & -1 & 1 & -1 & 1 & 1 & -1 \end{pmatrix} \quad \text{или} \quad \begin{pmatrix} 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 & 0 & 1 & 0 & 1 \\ 1 & 1 & 0 & 0 & 0 & 0 & 1 & 1 \\ 1 & 0 & 0 & 1 & 0 & 1 & 1 & 0 \end{pmatrix}$$

FIG.13

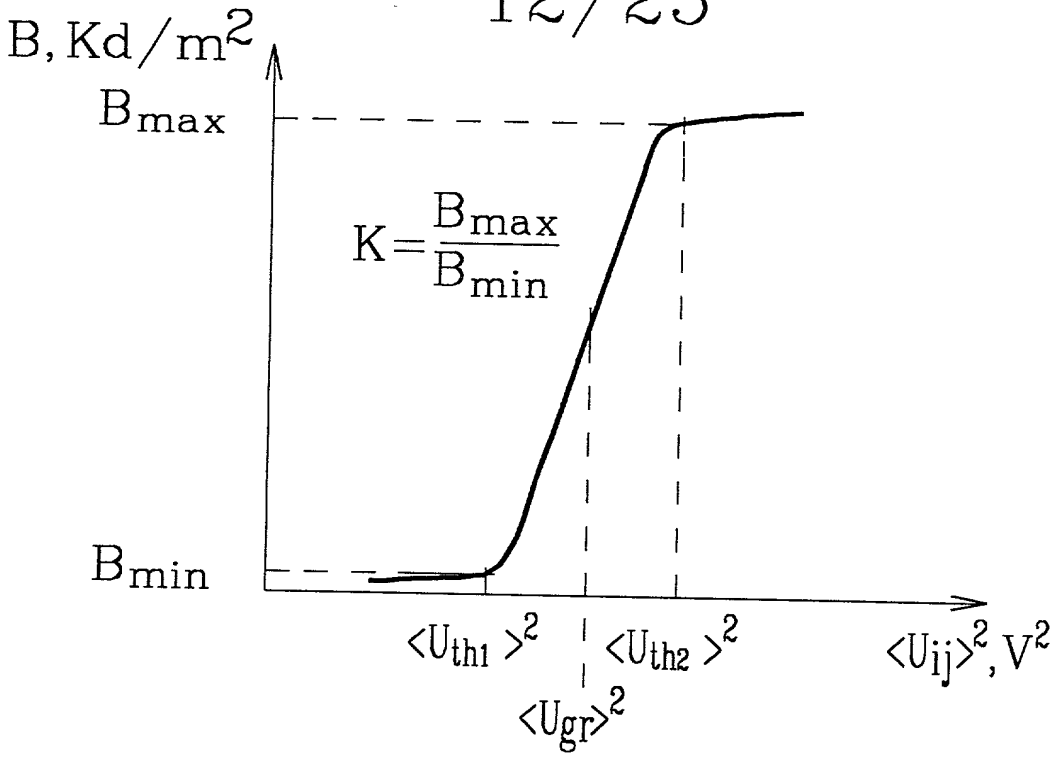

FIG.14

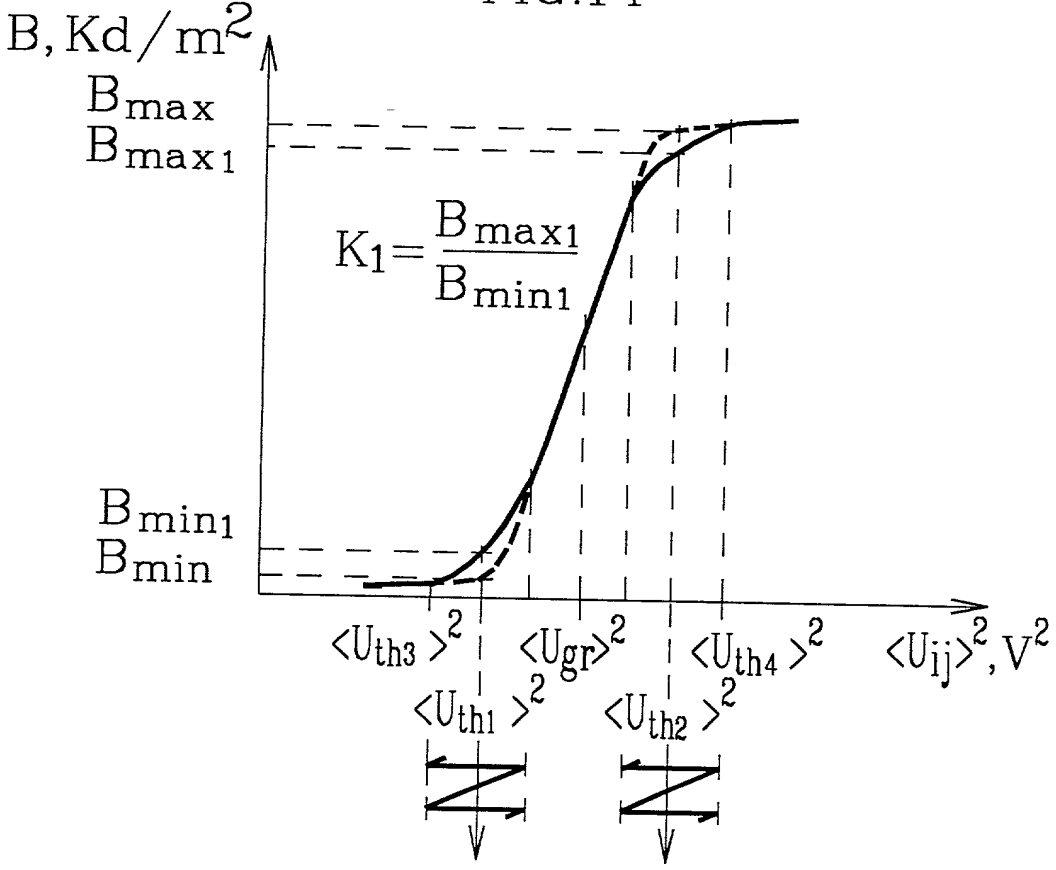

FIG.15

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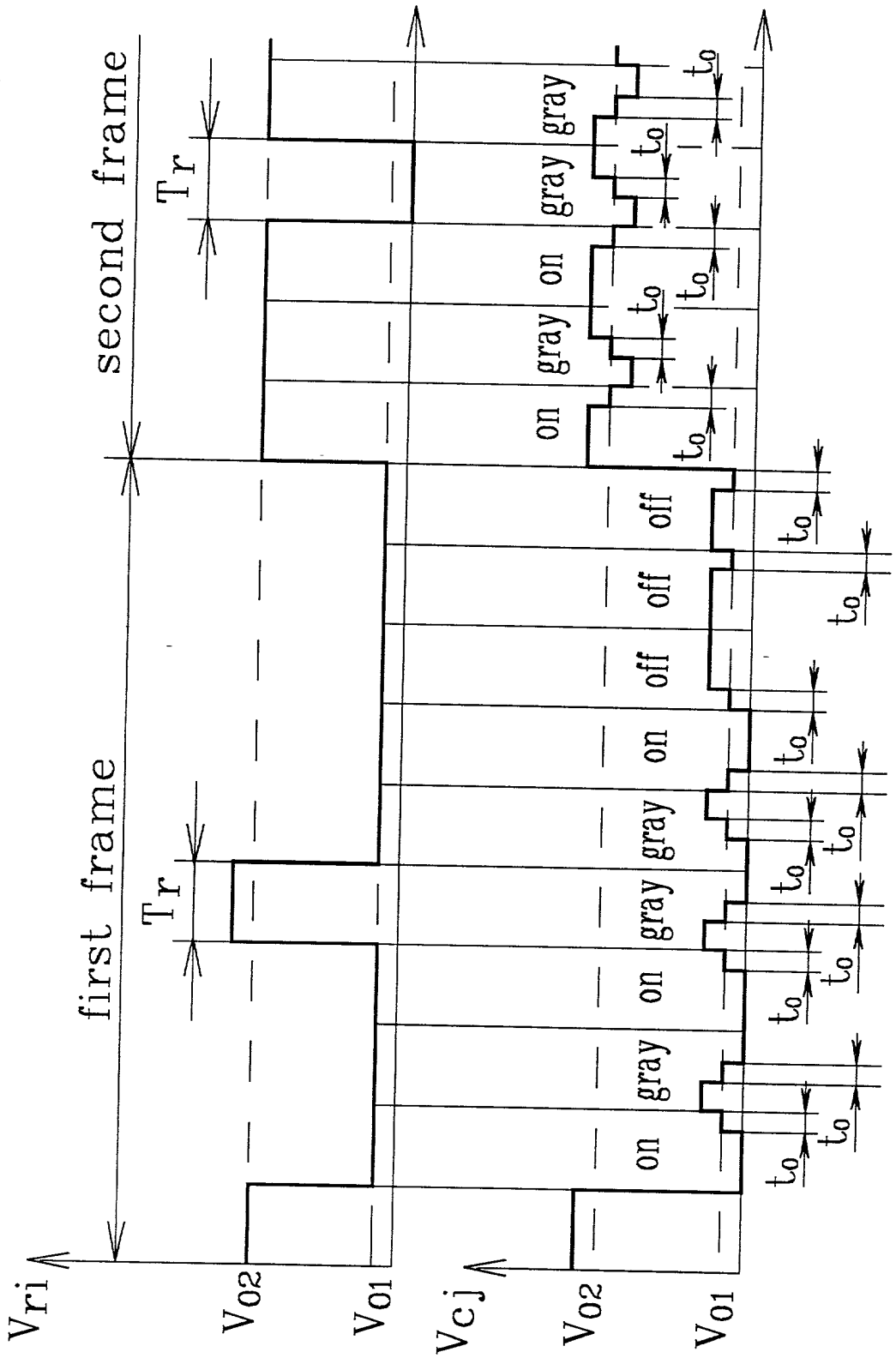

FIG.16

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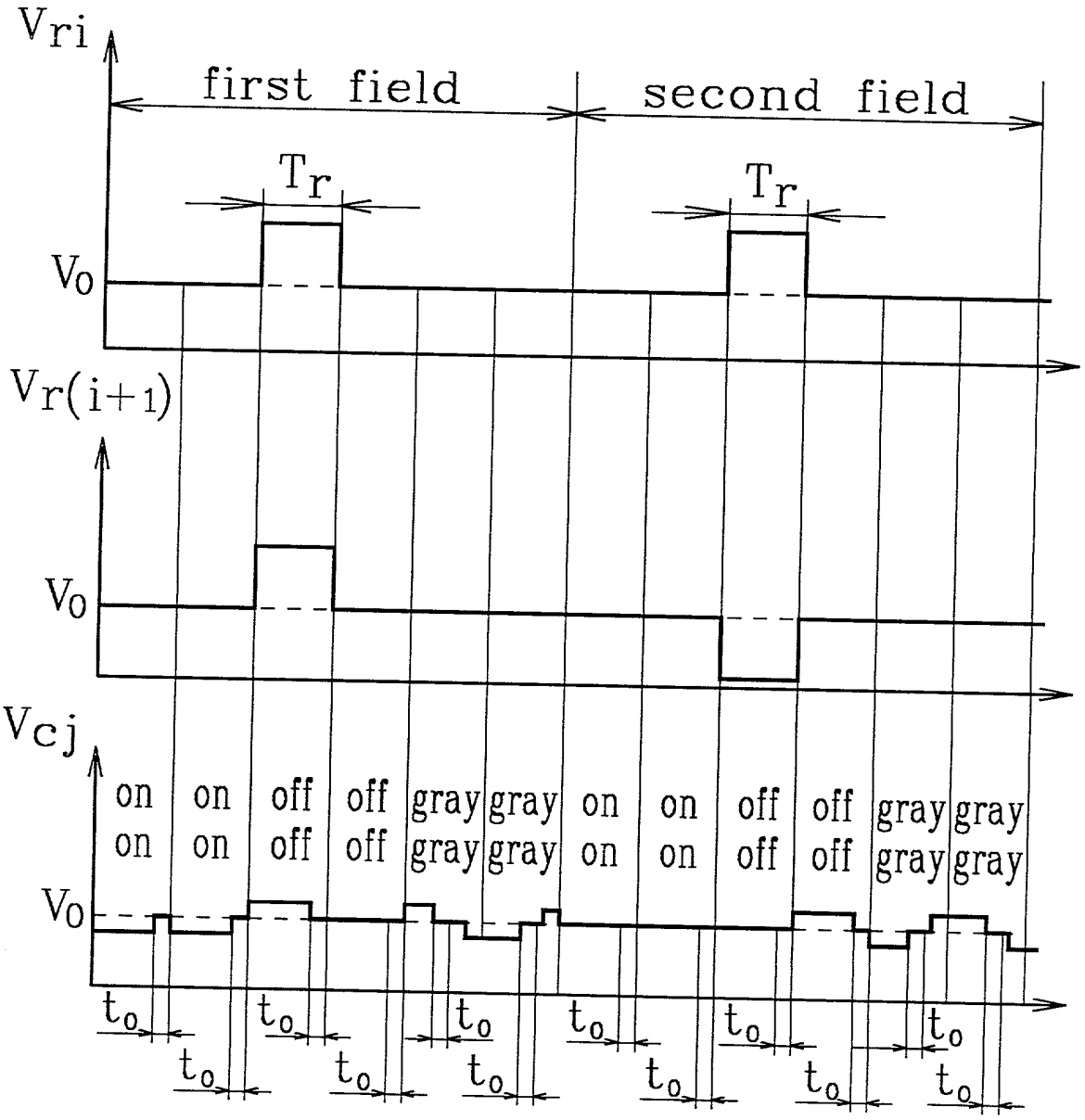

FIG.17

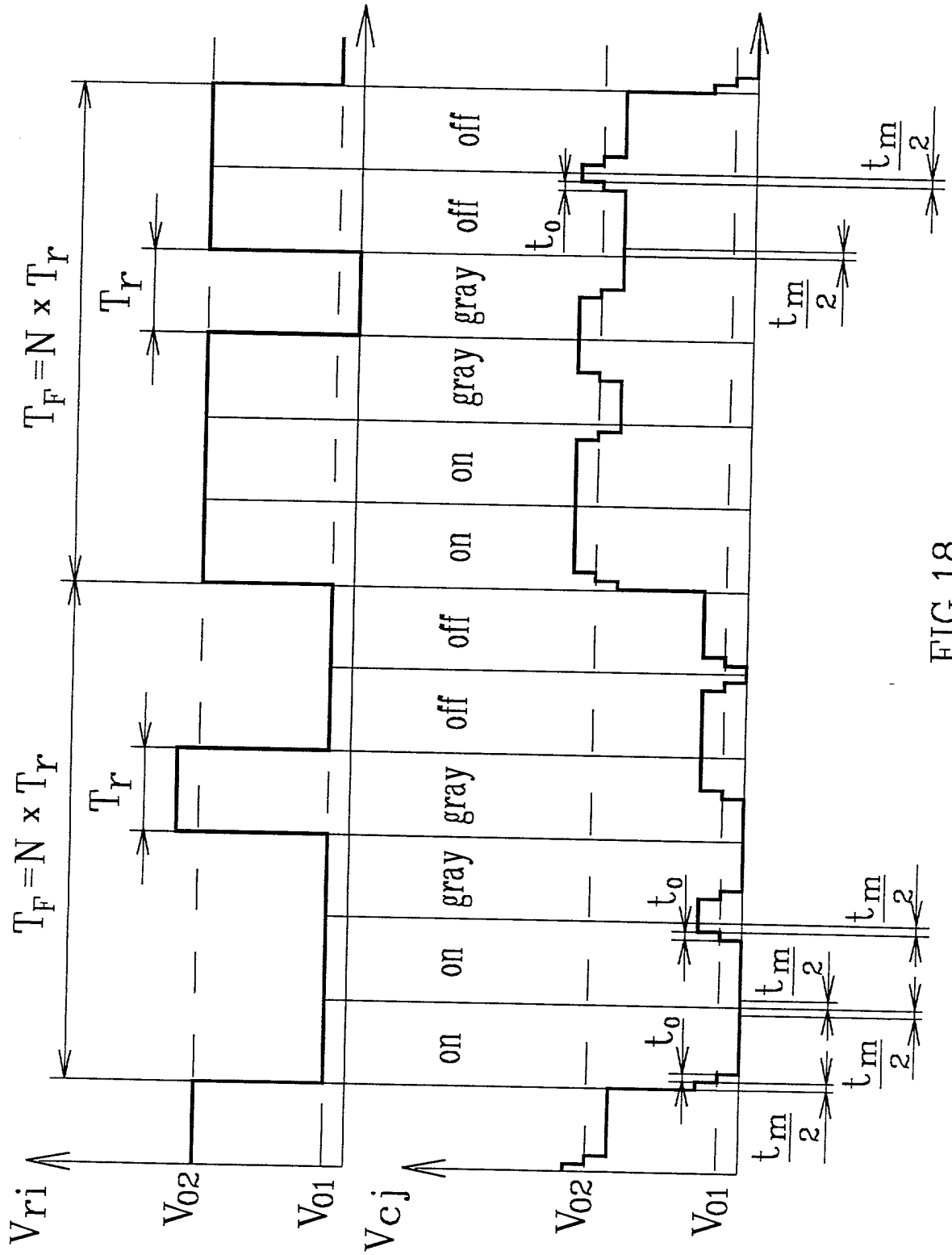

FIG.18

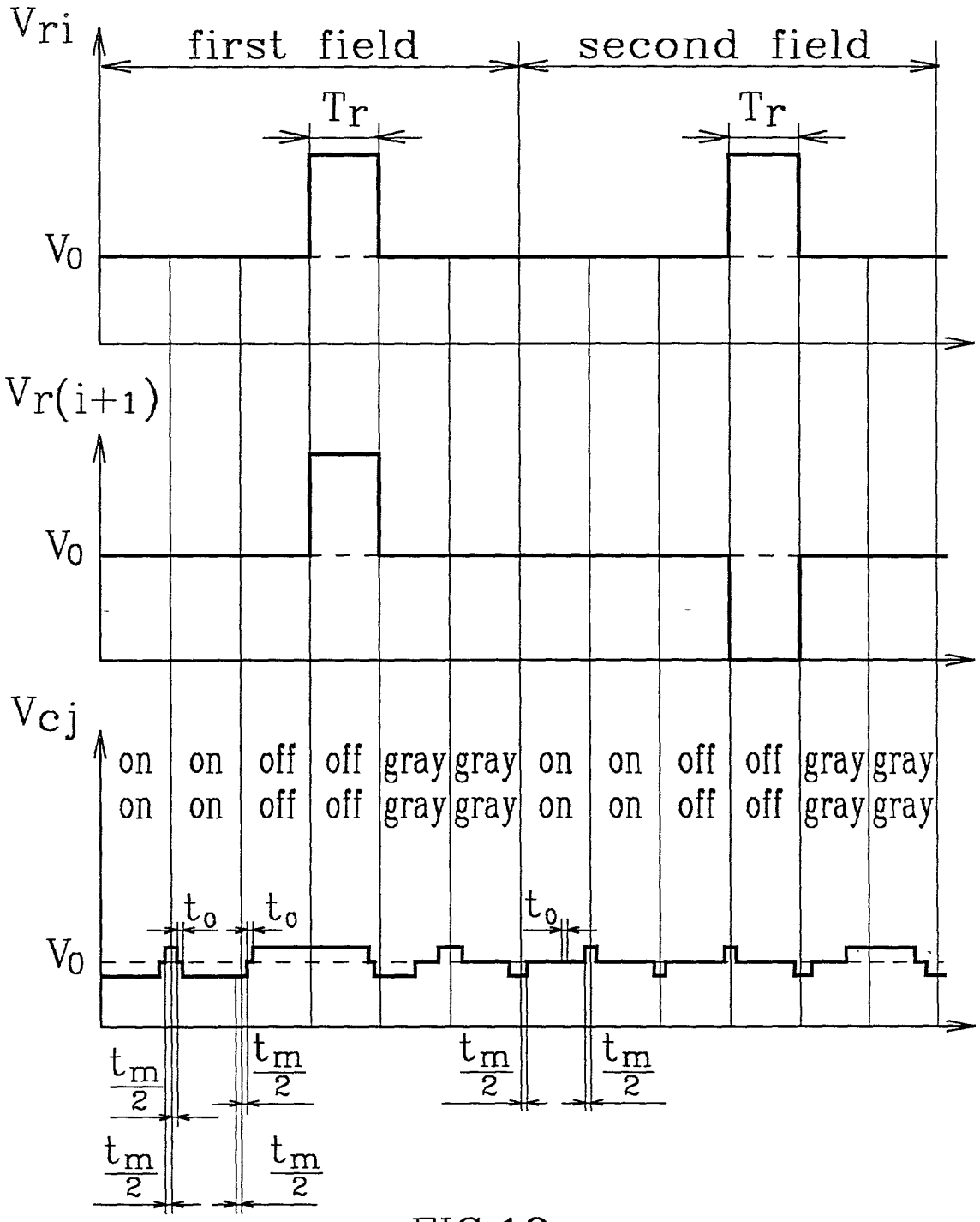
Vri
first field
second field
Tr
Tr
Vo
Vr(i+1)
Vo
Vcj
on on off off gray gray on on off off gray gray
on on off off gray gray on on off off gray gray
to
to
to
Vo
tm/2
tm/2
tm/2
tm/2
tm/2
tm/2

FIG.19

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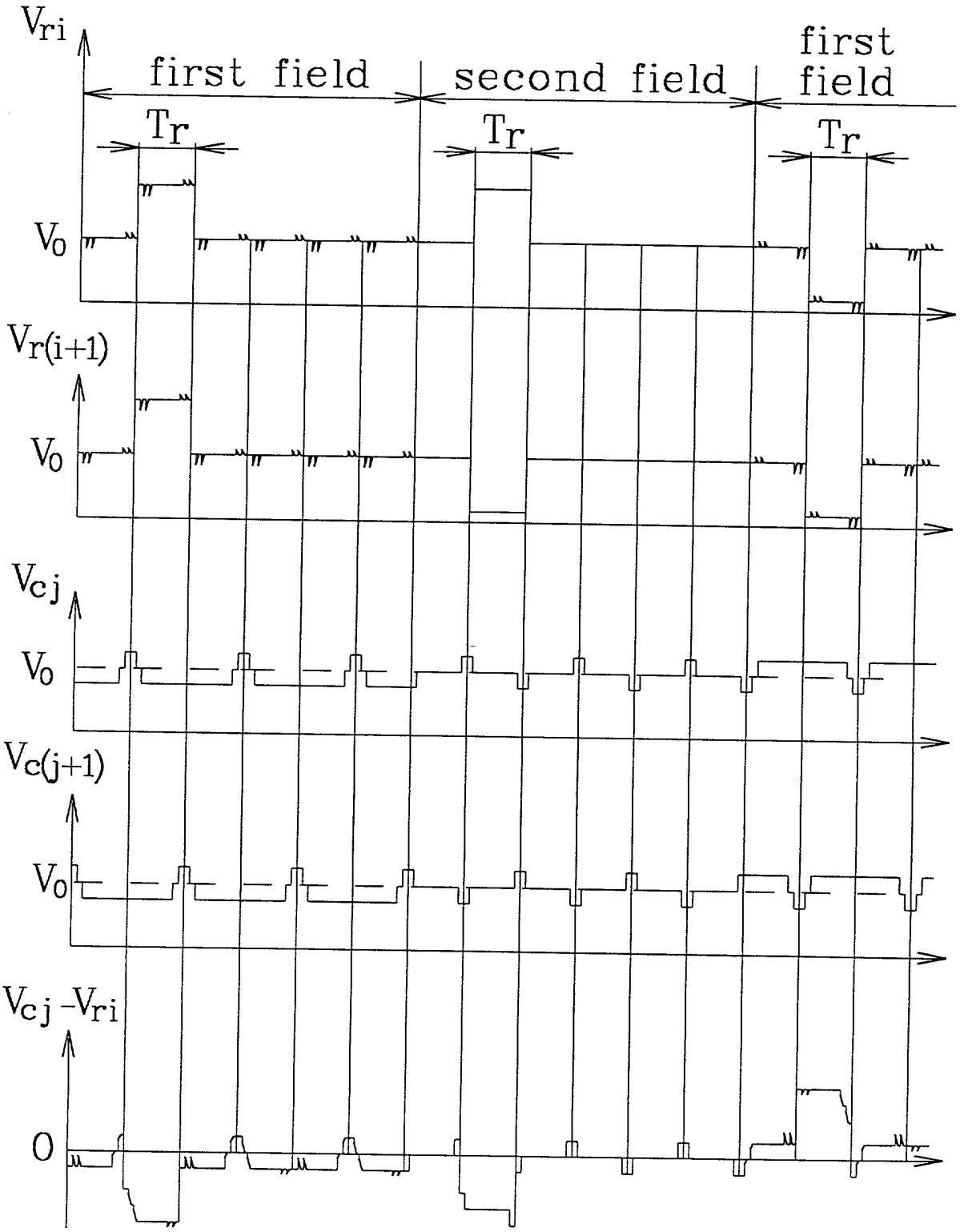

FIG. 20

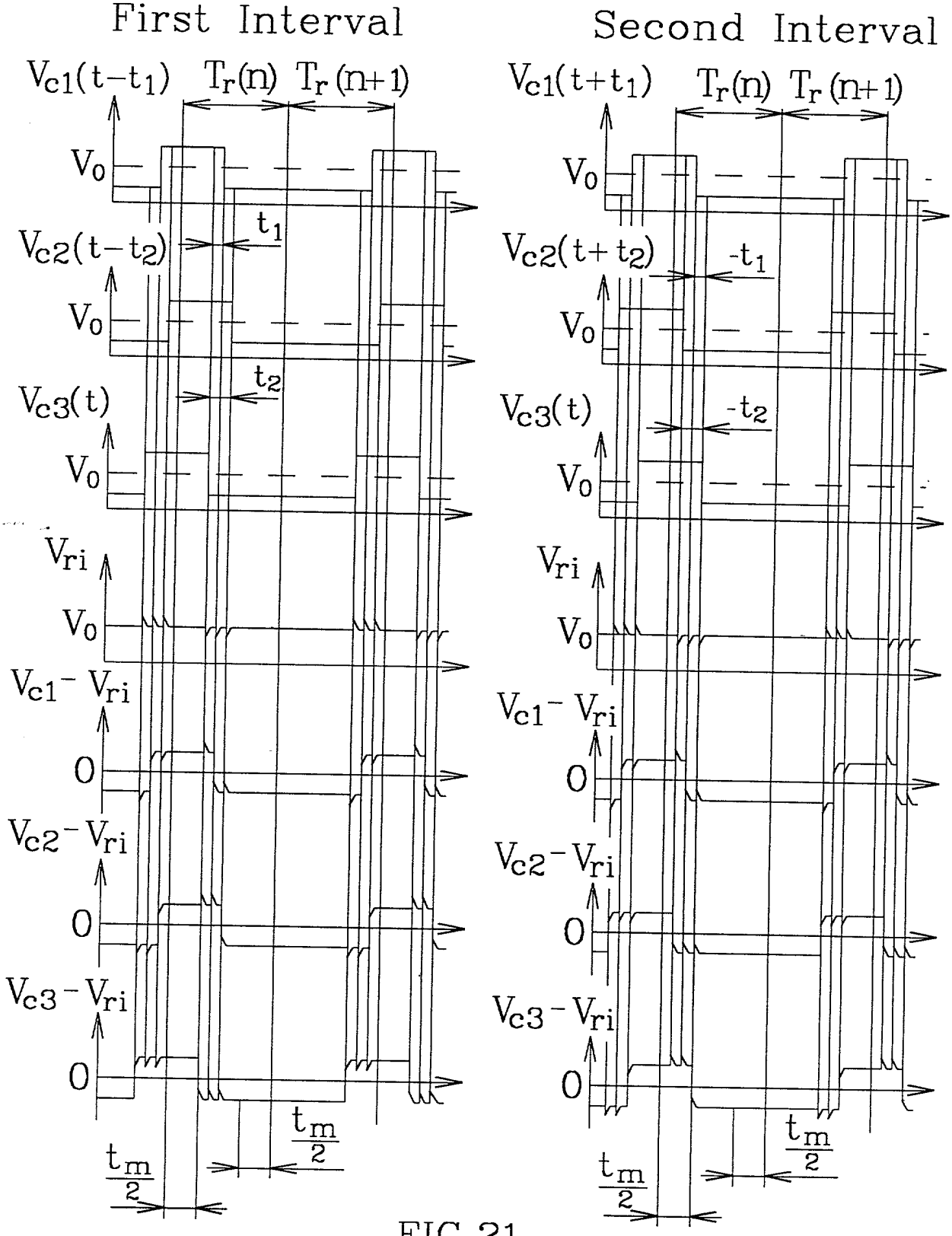

FIG.21

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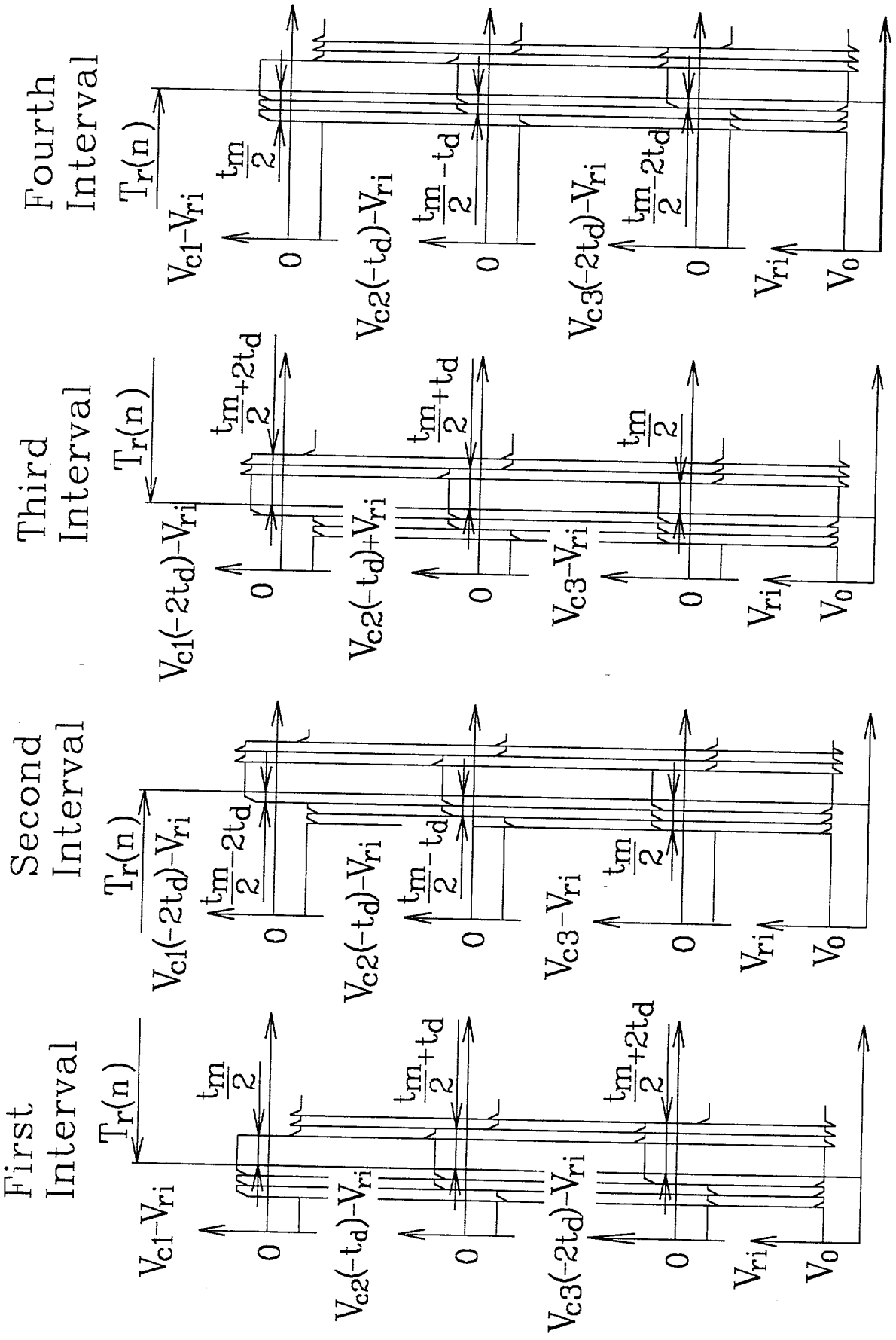

FIG.22

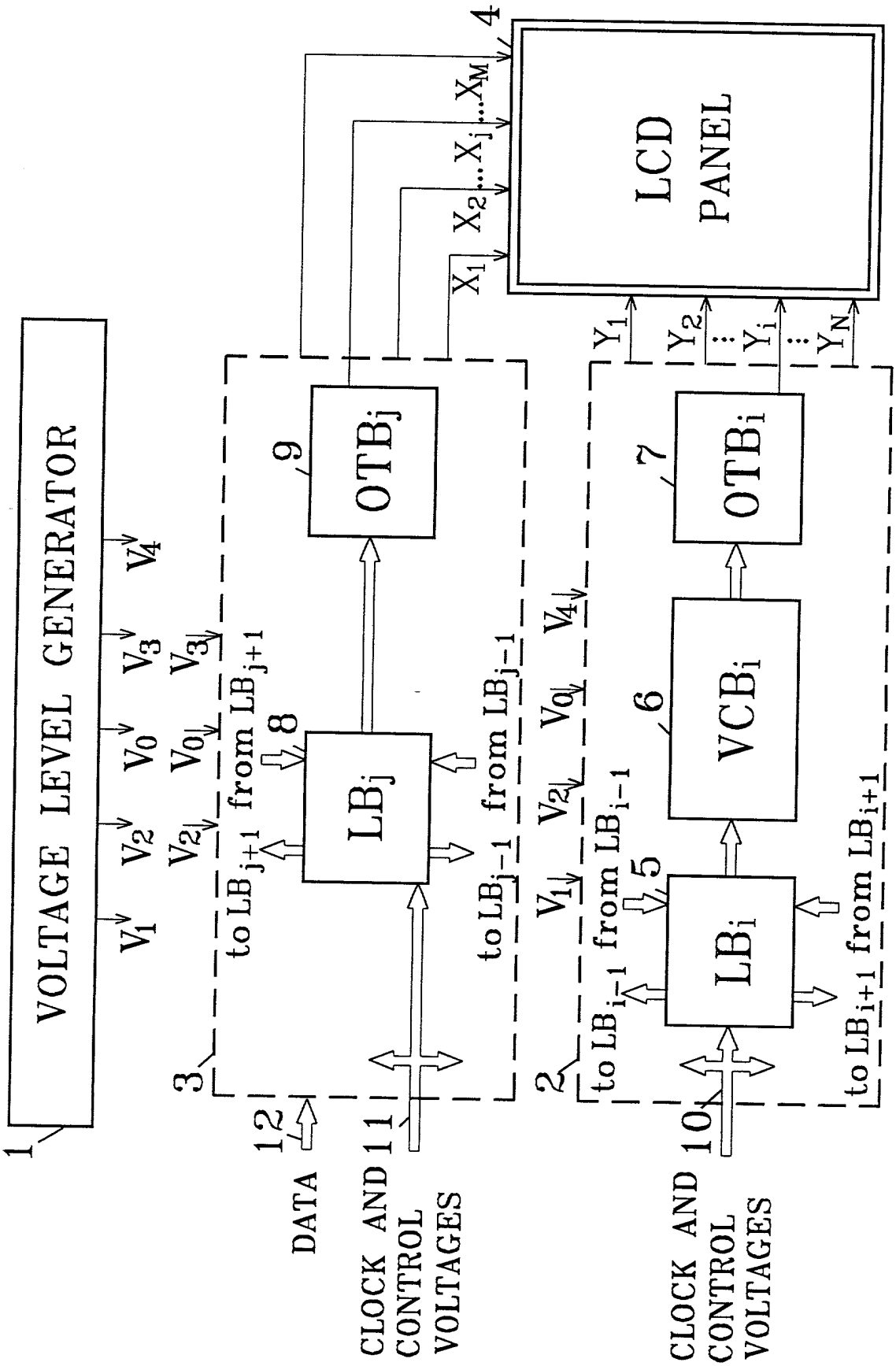

FIG.23

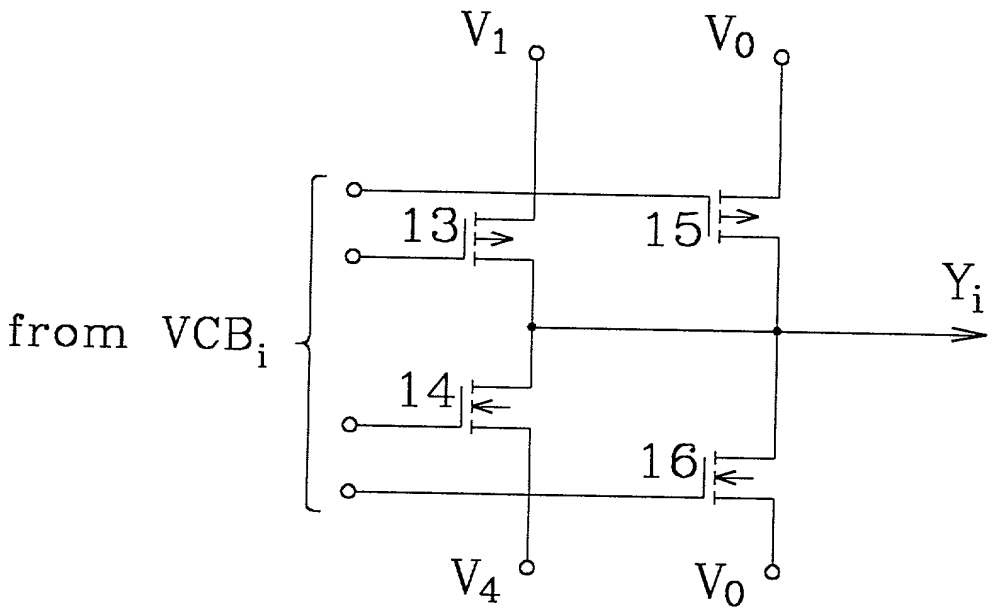

FIG.24

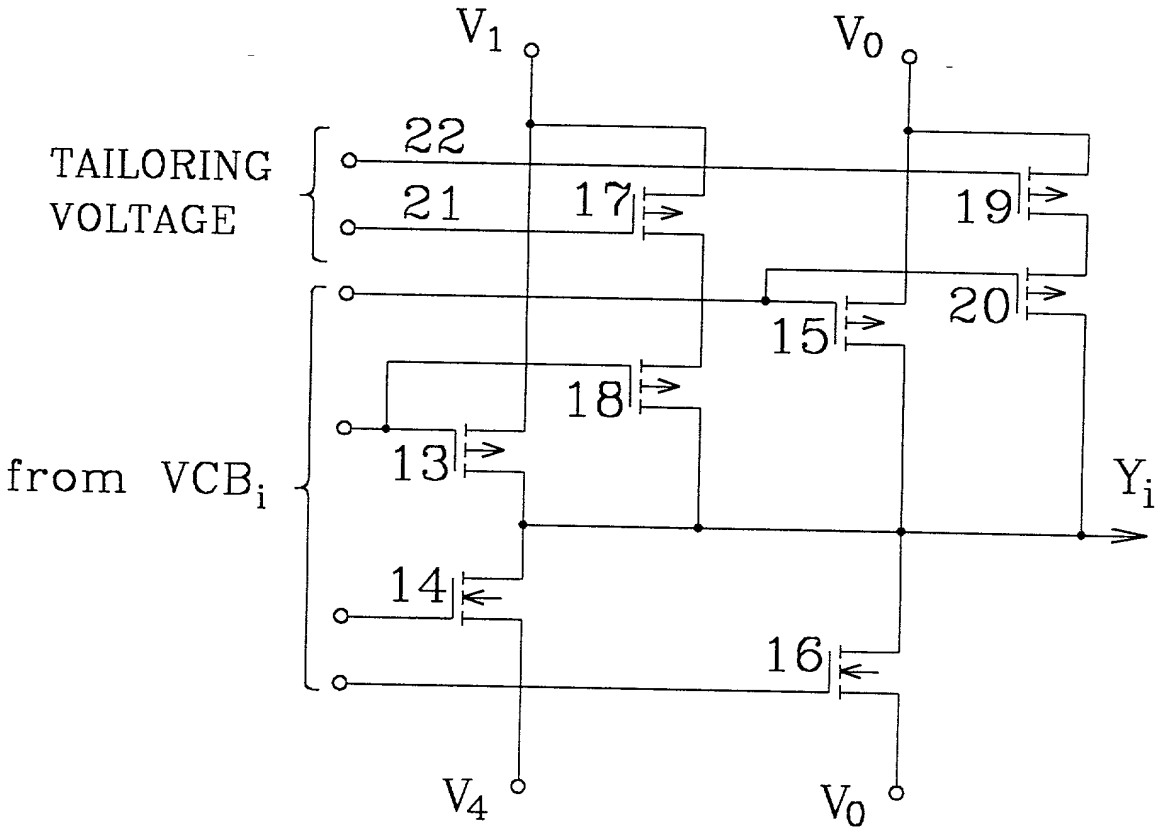

FIG.25

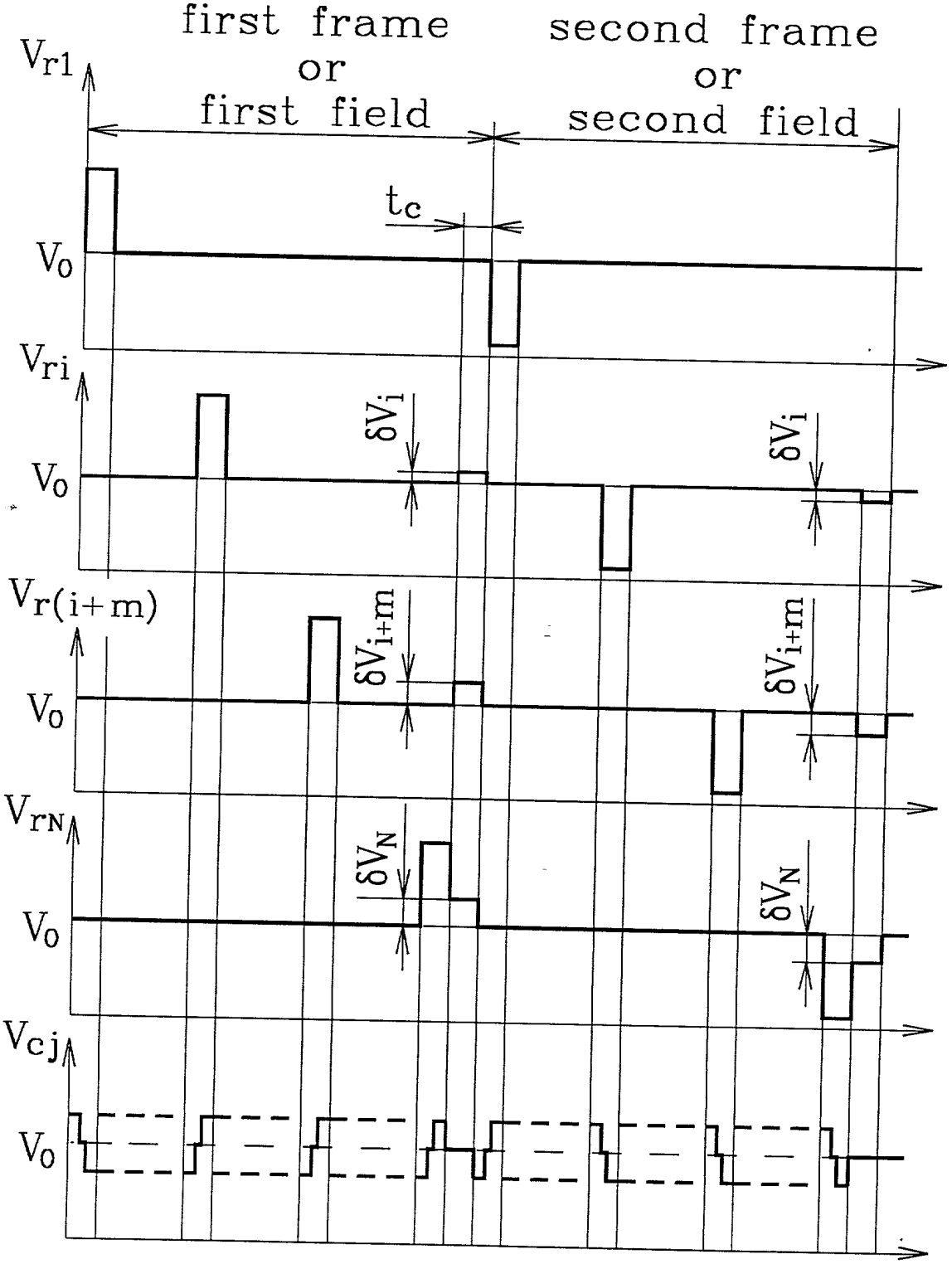

FIG.26

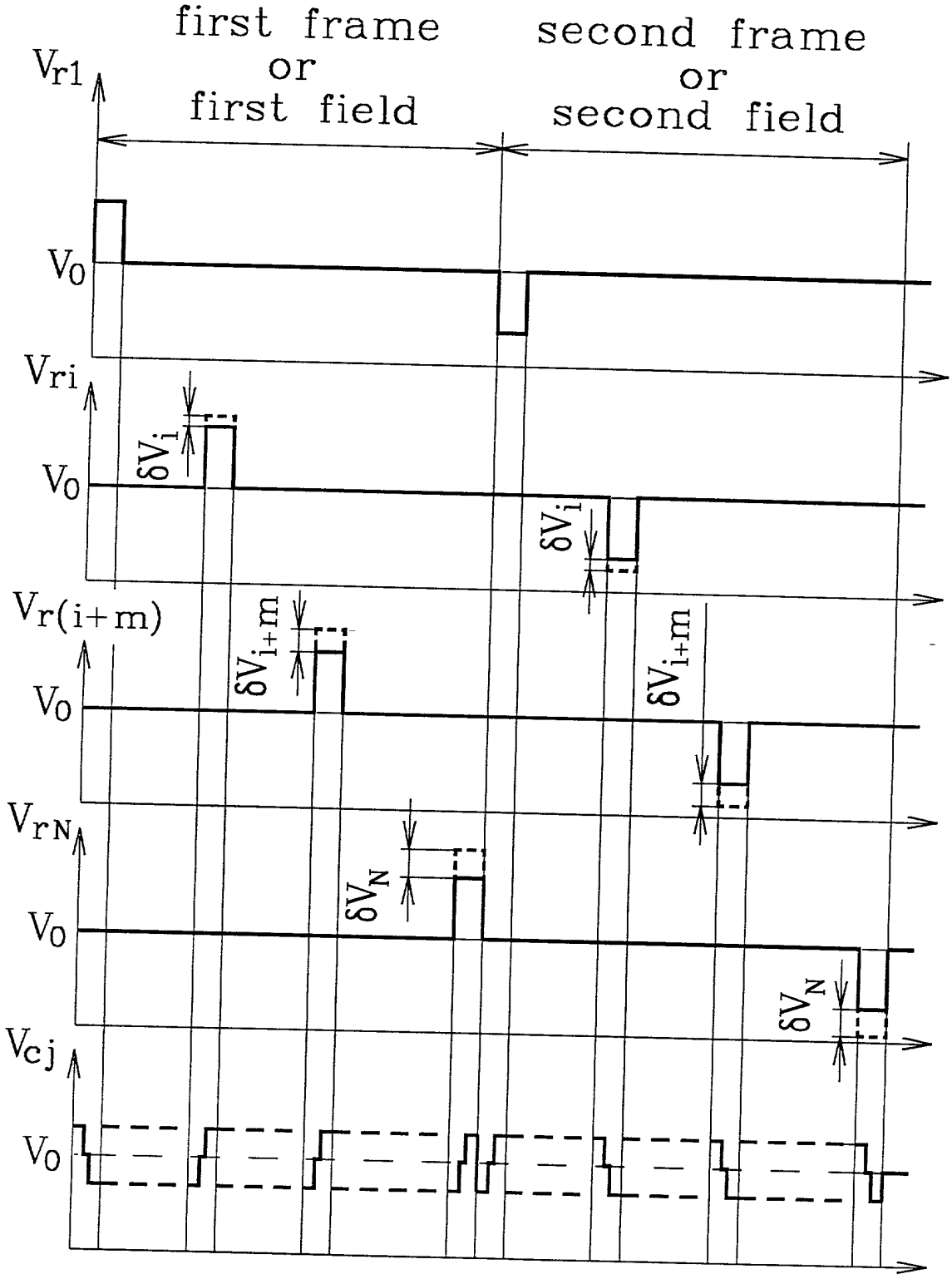
first frame
or
first field
second frame
or
second field
Vr1
V0
Vri
δVi
V0
δVi
Vr(i+m)
δVi+m
δVi+m
V0
VrN
δVN
V0
δVN
Vcj
V0

FIG. 27

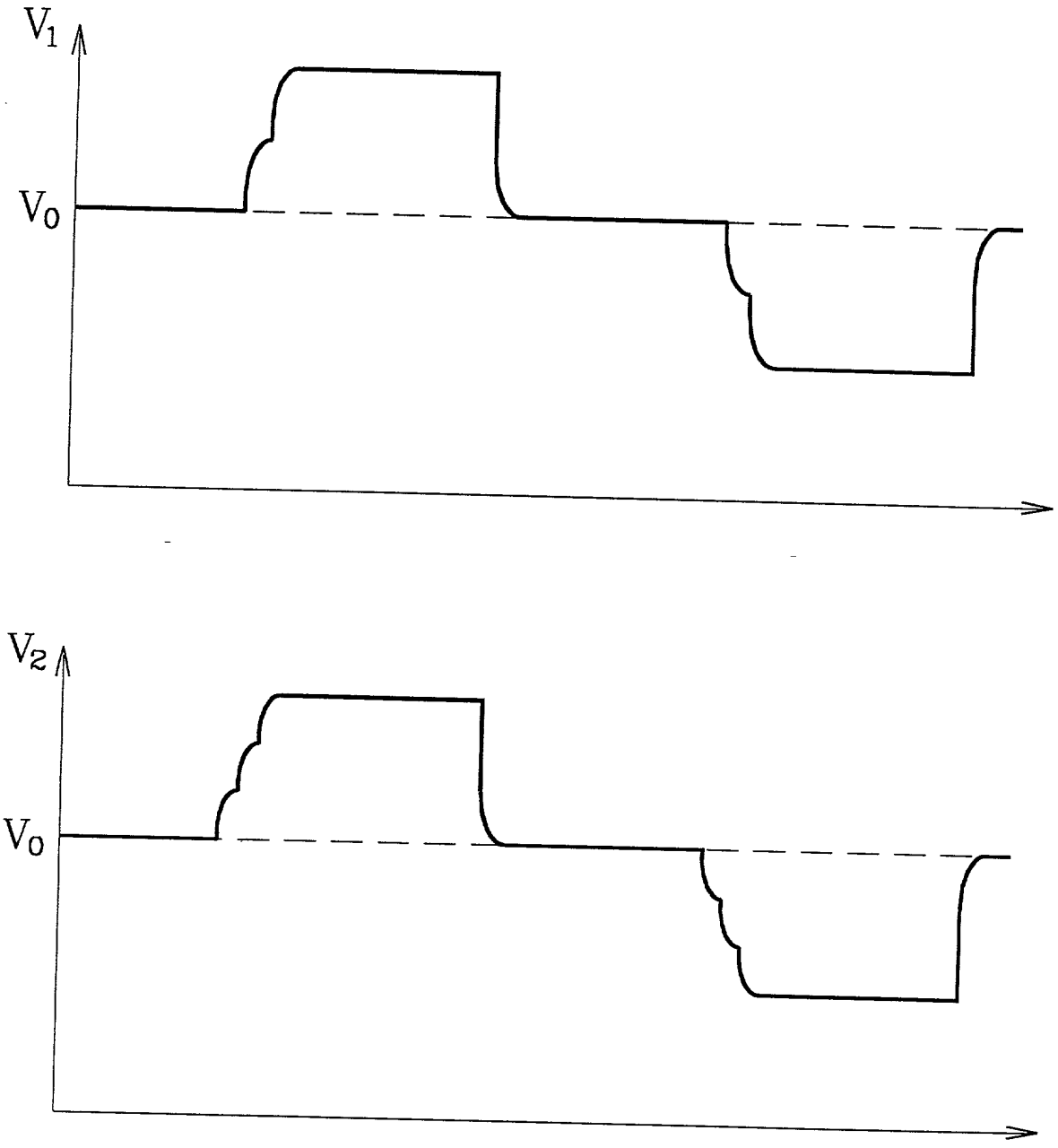

FIG.28

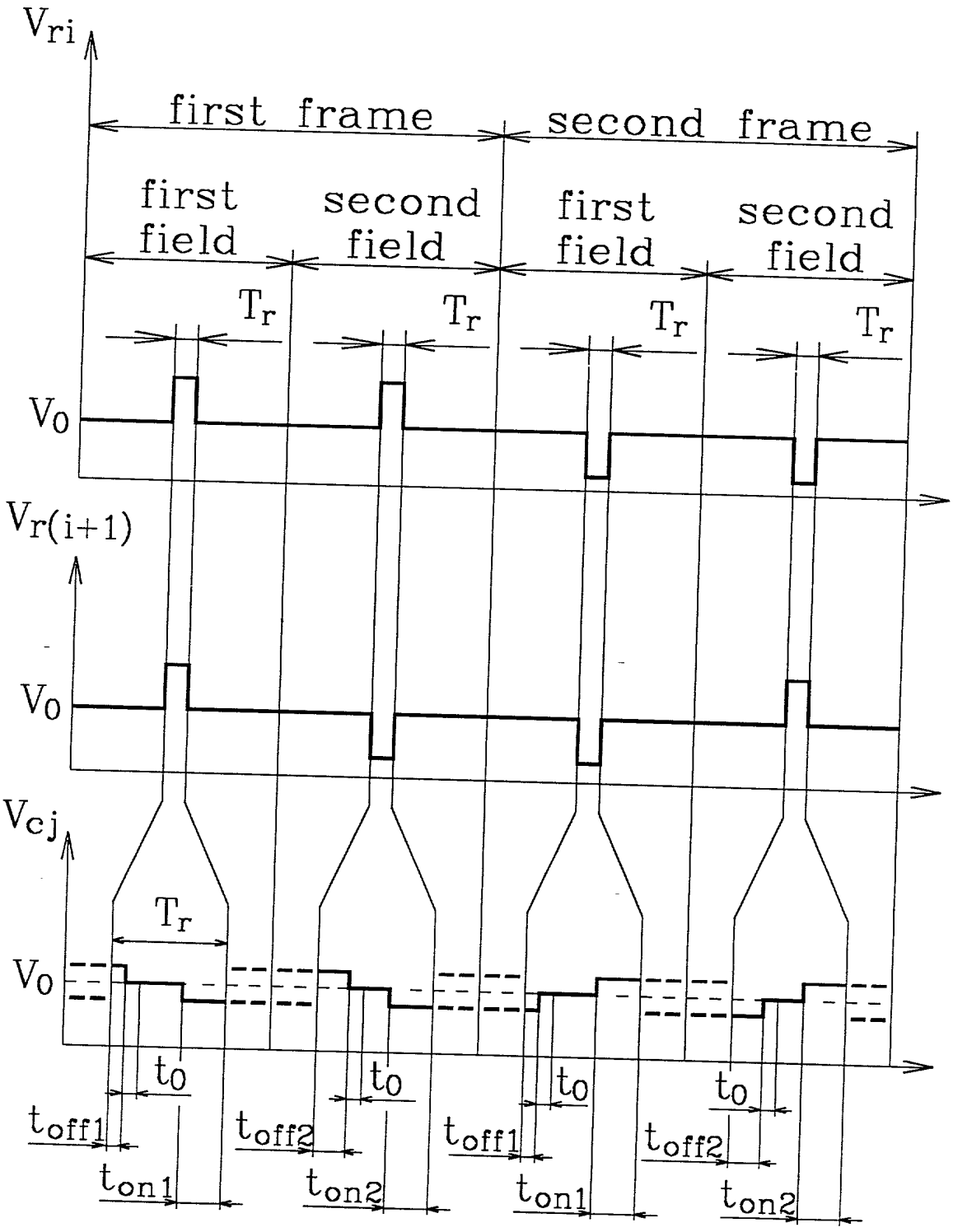
Vri
first frame
second frame
first field
second field
first field
second field
Tr
Tr
Tr
Tr
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FIG. 29

SOLE/JOINT

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name: that I verily believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter claimed and for which a patent is sought in the application entitled:

which application is:
☐ the attached application
(for original application)

☐ Application No. _____
(Confirmation No.) filed
and amended on _____

(for declaration not accompanying application)

that I have reviewed and understand the contents of the specification of the above-identified application, including the claims, as amended by any amendment referred to above; that I acknowledge my duty to disclose information of which I am aware and which is material to the patentability of this application as defined in 37 C.F.R. 1.56, that I hereby claim priority benefits under Title 35, United States Code §119(a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate. §119(c) of any United States provisional application(s), or §365(a) of any PCT International application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate or of any PCT International application having a filing date before that of the application on which priority is claimed:

Application Number	Country	Filing Date	Priority Claimed Yes	Priority Claimed No
			☐	☐

I hereby claim the benefit under 35 United States Code §120 of any United States application(s), or §365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in a listed prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge my duty to disclose any information material to the patentability of this application as defined in 37 C.F.R. 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application No.	Filing Date	Status

I hereby appoint John H. Mion, Reg. No. 18,879; Thomas J. Macpeak, Reg. No. ~~19,292~~; Robert J. Seas, Jr., Reg. No. 21,092; Darryl Mexic, Reg. No. ~~23,063~~; Robert V. Sloan, Reg. No. 22,775; Peter D. Olexy, Reg. No. ~~24,513~~; ~~J.~~ Frank Osha, Reg. No. ~~24,625~~; Waddell A. Biggart, Reg. No. 24,861; Louis Gubinsky, Reg. No. 24,835; Neil B. Siegel, Reg. No. 25,200; David J. Cushing, Reg. No. ~~28,703~~; John R. Inge, Reg. No. 26,916; Joseph J. Ruch, Jr., Reg. No. 26,577; Sheldon I. Landsman, Reg. No. 25,430; Richard C. Turner, Reg. No. ~~29,710~~; Howard L. Bernstein, Reg. No. 25,665; Alan J. Kasper, Reg. No. 25,426; Kenneth J. Burchfiel, Reg. No. ~~31,333~~; Gordon Kit, Reg. No. 30,764; Susan J. Mack, Reg. No. 30,951; Frank L. Bernstein, Reg. No. 31,484; Mark Boland, Reg. No. 32,197; William H. Mandir, Reg. No. 32,156; Brian W. Hannon, Reg. No. 32,778; Abraham J. Rosner, Reg. No. ~~33,276~~; Bruce E. Kramer, Reg. No. ~~33,725~~; Paul F. Neils, Reg. No. 33,102; Brett S. Sylvester, Reg. No. 32,765; Robert M. Masters, Reg. No. 35,603, George F. Lehnigk, Reg. No. 36,359, John T. Callahan, Reg. No. 32,607, Steven M. Gruskin, Reg. No. 36,818, Peter A. McKenna, Reg. No. 38,551 and Edward F. Kenehan, Reg. No. 28,962, my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and request that all correspondence about the application be addressed to **SUGHRUE, MION, ZINN, MACPEAK & SEAS, PLLC**, 2100 Pennsylvania Avenue, N.W., Washington, D.C. 20037-3213.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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